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Multi-level converter topologies for low voltage drives

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Abstract

Inverters synthesizing output voltages consisting of two levels, commonly known as two-level inverters, have dominated the global market for a long time. Today, further emphasis is being put on inverter efficiency and power quality. One way of improving these aspects is to use an inverter synthesizing a staircase voltage waveform consisting of three or more levels. Such inverters are known as multi-level inverters.

The thesis begins by pointing out key differences as well as advantages and disadvantages of two-level and multi-level inverters. The different multi-level inverter topologies are presented and the decision to further investigate the diode clamped inverter motivated. The diode clamped multi-level inverter and its related control circuit are discussed in detail.

Then, simulations containing the two-level inverter and the diode clamped inverter are explained, carried out and eventually used to confirm the alleged advantages and disadvantages, and to show that the diode clamped inverter is more flexible, yielding both better inverter efficiency and power quality. Finally, cost, weight and space requirements of the two inverters are compared to provide a full comparison.

Keywords: Multi-level, Inverter, Converter, Low voltage, IGBT, Loss-estimation

Sammanfattning

Omvandlare som syntetiserar spänningar bestående av två nivåer, vanligen benämnda tvånivåomvandlare, har dominerat den globala marknaden länge. I dagsläget finns en ökande efterfrågan på förhöjd verkningsgrad och elkvalitet, och ett sätt att i ett system förbättra dessa egenskaper kan vara att använda en omvandlare som syntetiserar trappstegsformade spänningar bestående av tre eller flera nivåer. Denna typ av omvandlare kallas flernivåomvandlare.

Uppsatsen börjar med att peka ut fundamentala skillnader samt för- och nackdelar mellan två- och flernivåomvandlare. De olika flernivåomvandlartopologierna presenteras och valet att vidare undersöka diode clamped-omvandlaren motiveras. Därefter diskuteras den valda omvandlaren och dess kontrollkrets i detalj.

Efter det beskrivs och används simuleringar innehållande båda typer av omvandlare för att visa på de i början av uppsatsen påstådda för- och nackdelarna med flernivåomvandlaren. Simuleringarna används också för att visa på att flernivåomvandlaren är en mer flexibel lösning som både ger bättre verkningsgrad och elkvalitet. I slutet av uppsatsen görs även en jämförelse med avseende på kostnad-, vikt- och platskrav för att ge en helhetsjämförelse.

Nyckelord: Flernivå, Växelriktare, Omvandlare, Lågspänning, IGBT, Förlustuppskattning

Foreword

First, I would like to thank my thesis supervisor and teacher Per Karlsson for his advice and excellent guidance, without which the end result would not have been what it is, throughout my thesis work.

I would like to thank Per Södergård, my supervisor at CG Drives & Automation. Per has, despite a tight schedule, always managed to find time for discussion and help.

The staff at CG Drives & Automation have constantly been very friendly and open with me. This has made my experience a pleasure and is greatly acknowledged.

I would also like to thank my examiner and teacher Mats Lilja for his comments on my work and for all interesting discussions that we have had during my time at LTH Campus Helsingborg, they will be missed.

Finally, I would like to express gratitude to my friends and family for their support and patience during this time.

Max F. Collins

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1 Introduction

1.1 Background

Recent studies have shown that, globally, electric motor-driven systems, EMDS, consume more than half of all electricity generated. In Swedish industry, EMDS account for around two thirds of the total consumption. EMDS are thus by far the largest source of electricity consumption and it is therefore of interest to ensure that these are operated efficiently [1, 2].

One way to improve efficiency is the use of variable speed drives, VSD. These drives match the speed and torque of the motor to that of the load, controlling the amount of power fed into the machine [1, 2].

CG Drives & Automation has over the last decades been successful in the field of control and monitoring of electrical motors. VSD for induction motors for voltages up to 690 VAC, low voltage, in the power range up to several MW have been developed in house. The topology used in these drives is a voltage source inverter, VSI, in which each leg can have two output voltage levels. This topology is, and has been, the dominating topology in the market for a very long time. A simplified two-level inverter circuit is shown below.

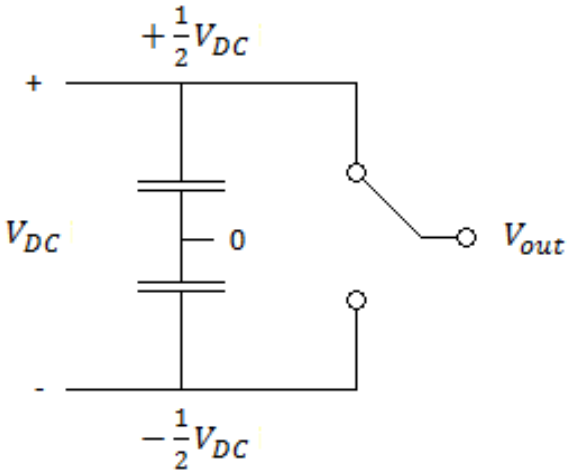

Fig 1.1 Simplified two-level inverter circuit.

When the switch is up, the output voltage ($V_{out} - V_0$) is $+\frac{1}{2}V_{DC}$. In the same way, when the switch is down, the output voltage is $-\frac{1}{2}V_{DC}$. By alternating

between these two switch states, an AC output voltage is synthesized. Clearly, since only two output voltages are allowed, the quality of the output waveform is determined by the switching frequency.

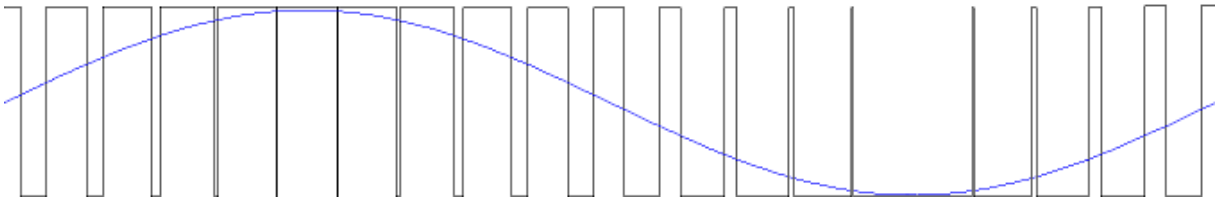

Fig 1.2 Output voltage waveform of a two-level inverter

Today, as mentioned above, more emphasis is being put on efficiency and power quality. A possible means of improvement could be the use of a VSI built on a multi-level topology, in which each leg can have three or more output voltage levels.

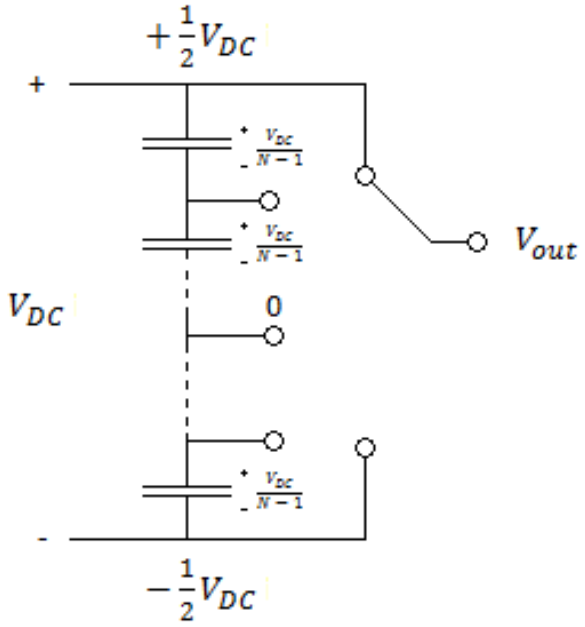

Fig 1.3 Simplified N-level inverter circuit

In an N-level inverter, N-1 capacitors split the dc bus voltage into N levels in incremental steps of $\frac{V_{DC}}{N-1}$. A combination of capacitor voltages are selected by the switch and thus form the output voltage. Again, by alternating between switch states, an AC output voltage is synthesized, but this time with N levels instead of just two. This means that the quality no longer is uniquely determined by the frequency, but also by amplitude.

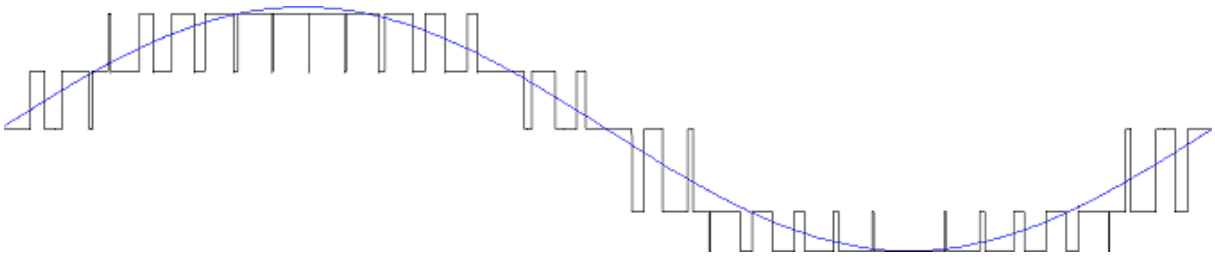

Fig 1.4 Output voltage waveform of a five-level inverter

The staircase waveform output by a multi-level inverter better approximates a sine wave, bringing a number of advantages.

- Less total harmonic distortion

  Closer approximation of a sine wave means less harmonic content. This makes possible a reduction (and in some cases even elimination) of the filter. If the reduction is significant, a smaller, lighter and cheaper end product which requires less space may be possible.

- Lower switching frequency

  For the same output power, a lower switching frequency is required. Less switching means less switching losses, giving a direct increase in efficiency.

- Less stress

  In a two-level inverter where each leg outputs either $+\frac{1}{2}V_{DC}$ or $-\frac{1}{2}V_{DC}$, each switching action means a change in voltage of V_{DC}. For high voltages and high switching frequencies, often needed when operating two-level inverters, this means high $\frac{dv}{dt}$ stresses on components. With a staircase waveform each step is much smaller, stressing each component less.

- Less voltage per component

  The way multi-level inverters are designed, there is less voltage across each switch. Thus, it may be possible to choose semiconductor devices with lower voltage ratings and thus better performance in other important areas.

Unfortunately, multi-level inverters, by the way they are designed, require a large number of semiconductor devices. This gives rise to a number of drawbacks compared to a two-level inverter:

- Increased complexity

  With additional semiconductor devices, a more advanced modulator will be needed in order to operate the circuitry.

- Increased weight, cost and space

  Each component added is associated with additional cost, weight and space.

1.2 Objectives

The main objective of this thesis is to identify multi-level inverter topologies suitable for use in low voltage drives and to evaluate the advantages and drawbacks associated with each topology as compared to the standard two-level voltage source inverter topology in terms of

- Efficiency
- Power quality
- Cost
- Weight
- Complexity
- Performance

A secondary objective is to analyse which topologies are suited for use as active front-end units in back-to-back arrangements.

1.3 Methodology

The primary methods used to assess the qualities of the inverter circuits are

- Literature studies
- Interviews
- Simulations

1.4 Expected Result

An orientation and recommendation on the possibilities of using multi-level inverter topologies in low voltage drives.

1.5 Outline of Thesis

This chapter serves as a short introduction to the thesis and introduces the concept of multi-level inverter topologies as well as their advantages and drawbacks as compared to the standardized two-level inverter topology.

The different multi-level inverter topology families are discussed in chapter 2. Provided is also motivation behind the choice to further investigate the diode clamped multi-level inverter topology. The theory and working principle of this particular topology is the topic of chapter 3.

In this thesis two systems are simulated. Common to both systems are the grid, a three phase uncontrolled rectifier and an induction motor to pose as load. The first system is a representation of the existing system and thus contains a three phase two-level inverter. It serves as a reference point against which all comparisons are to be made. The second system contains a three phase three-level diode clamped inverter and constitutes the system to be investigated. Chapter 4 introduces the systems and presents all simulation results.

Inverter cost and weight concerns are addressed in chapter 5.

The results are summarized and the thesis concluded in chapter 6.

2 Multi-level Inverters

Today, there are three main groups of multi-level inverters – diode clamped inverters, flying capacitor inverters, and cascaded H-bridge inverters [3]. The advantages and disadvantages of each group are considered.

2.1 Diode Clamped Multi-level Inverter

A five-level diode clamped inverter is shown below. Here, one dc voltage source, V_{DC}, is used and split into five voltage levels ($\pm\frac{V_{DC}}{2}$, $\pm\frac{V_{DC}}{4}$ and 0) by the series capacitors. Each level can then be connected to the output through use of the switches.

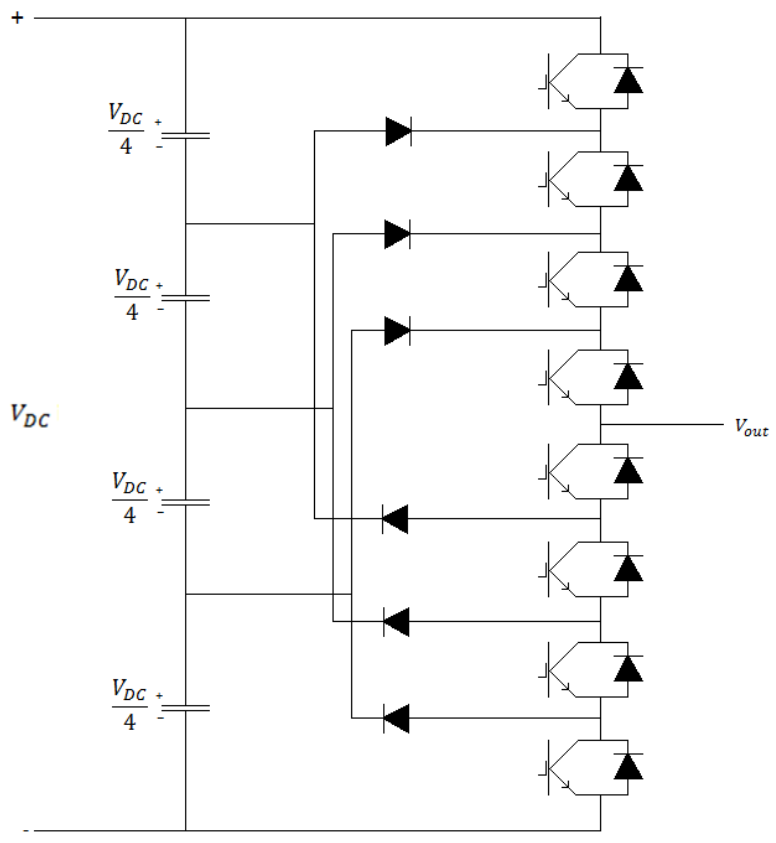

Fig 2.1 One leg of a five-level diode clamped inverter

Fundamental to this topology are the clamping diodes used to clamp the switches to the intermediate capacitors. This way, using the five-level inverter above as an example, no switch will experience voltages in excess of $\frac{V_{DC}}{4}$.

It should be pointed out that some of the clamping diodes for inverters with more than three levels will experience voltages in excess of that experienced by the main switches. Thus, if diodes with a voltage rating equal to that of the transistors are to be used, series connection of multiple diodes is necessary. While this solves the problem of the voltage ratings, it increases the number of clamping diodes from $2(N-2)$ per phase to that of $(N-1)(N-2)$ per phase [3].

Further, an N-level diode clamped inverter requires $N-1$ capacitors to split the voltage and $2(N-1)$ switch pairs per phase. Table 2.1 below summarizes the total number (three phases) of dc bus capacitors, clamping diodes and switch pairs needed for inverters with 3, 5, 7 and 9 intermediate levels [3].

	# levels in V_{LL}	**# levels in V_{LN}**	**# dc bus capacitors**
3	5	9	2
5	9	17	4
7	13	25	6
9	17	33	8
	# clamping diodes	**# switch pairs**	**# switch states**
3	6	12	27
5	36	24	125
7	90	36	343
9	168	48	729

Table 2.1.

Note that all phase legs share a common dc bus and that no other capacitors are used in this topology. This fact is a distinct advantage of the diode clamped multi-level inverter as compared to the other topologies to be discussed. It minimizes the total capacitance requirements of the inverter, it allows the capacitors (since they are arranged in series) to be pre-charged as a group, and it makes the topology very much suited to back-to-back arrangements.

The fact that diode clamped multi-level inverters with more than three levels require series connection of clamping diodes complicates the design and raises

cost concerns. As such, diode clamped inverters with high number of levels are, at present time, cumbersome and often impractical.

In addition to increased circuit complexity, the intermediate dc levels must be maintained. This is a known problem for inverters of this kind with more than three levels.

2.2 Flying Capacitor Multi-level Inverter

The flying capacitor multi-level inverter was proposed as an alternative to the diode clamped inverter.

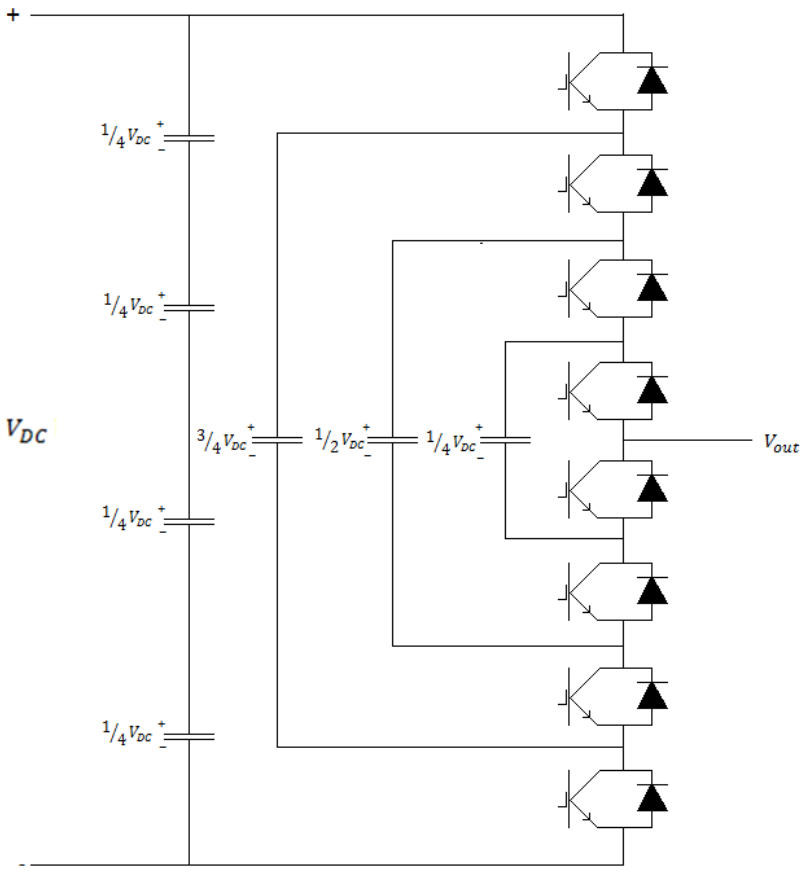

Fig 2.2 One leg of a five-level flying capacitor inverter

The structure of this inverter topology is very similar to that of the diode clamped inverter, the main difference being that capacitors are used as a replacement for clamping diodes.

One advantage of the flying capacitor topology as compared to the diode clamped topology is the fact that while having an equal number of switch

states, it has a much larger number of usable (and thus redundant) switch states. For instance, while a five-level diode clamped inverter only has one switch combination that outputs $^1/_4 V_{DC}$, a five-level flying capacitor inverter has four switch combinations that does the same. Redundant switch states can be incorporated in the control system in order to balance the intermediate dc levels, a persisting problem of diode clamped inverters of higher orders.

An N-level flying capacitor inverter requires $^1/_2 (N-1)(N-2)$ flying capacitors per phase, and $2(N-1)$ switch pairs per phase [3].

Table 2.2 below summarizes the total number (three phases) of dc bus capacitors, flying capacitors and switch pairs needed for inverters with 3, 5, 7 and 9 intermediate levels [3].

	# levels in V_{LL}	**# levels in V_{LN}**	**# dc bus capacitors**
3	5	9	2
5	9	17	4
7	13	25	6
9	17	33	8
	# flying capacitors	**# switch pairs**	**# switch states**
3	3	12	27
5	18	24	125
7	45	36	343
9	84	48	729

Table 2.2.

While the flying capacitors allow better and more flexible control of the intermediate dc levels, they are hard to pre-charge and are also more expensive and bulky (even though they are fewer) than clamping diodes. They also make the topology unfit for back-to-back arrangements.

2.3 Cascaded H-bridge Multi-level Inverter

This topology is based on series connection of a number of H-bridges.

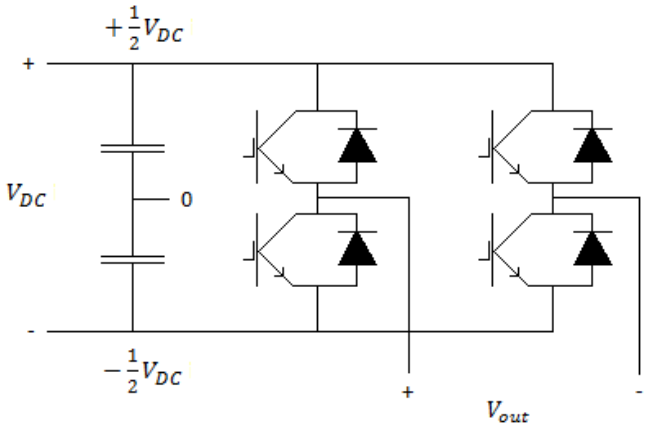

Fig 2.3 A single H-Bridge

An H-bridge can, through use of its switches, connect the output to $\pm {}^{1}/_{2}\, V_{DC}$

or 0. By cascading a number of H-bridges, the total output voltage then becomes the sum of the individual H-bridge output voltages.

This configuration shares many advantages with the flying capacitor topology. For instance, since V_{out} equals the sum of the individual H-bridge output voltages, $V_{out} = +V_{DC}$ can, in a 5-level inverter, be achieved through two different switch combinations. Similarly, $V_{out} = -V_{DC}$ can also be achieved through two different switch combinations. Thus, redundant switch states may be incorporated in the controller.

The fact that it is modular (constructed from a number of H-bridges) is also a positive design feature.

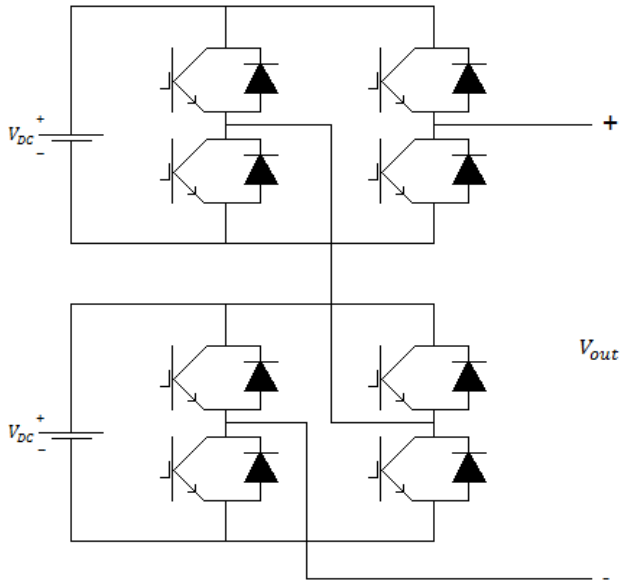

Fig 2.4 One leg of a 5-level cascaded H-bridge inverter

An N-level cascaded H-bridge inverter requires $^1/_2\,(N-1)$ isolated supplies

(capacitors or connections to secondary windings of a transformer) per phase. The number of switches per leg is calculated as $2(N-1)$ [3].

Table 2.3 below summarizes the total number (three phases) of dc bus capacitors, isolated supplies and switch pairs needed for inverters with 3, 5, 7 and 9 intermediate levels [3].

	# levels in V_{LL}	**# levels in V_{LN}**	**# isolated supplies**
3	5	9	3
5	9	17	6
7	13	25	9
9	17	33	12
	# switch pairs	**# switch states**	
3	12	27	
5	24	125	
7	36	343	
9	48	729	

Table 2.3.

The main disadvantage and limitation of this topology is the need for a large number of isolated voltage sources. For inverters with many levels, both these options are impractical for reasons already discussed.

2.4 Conclusions

Adding more levels to the output voltage of a voltage source inverter means adding more semiconductor devices and complementary components. Taking a flying capacitor multi-level inverter as an example, it is seen that the jump between three and five levels is a rather large one, requiring an additional 15 capacitors, 12 switch pairs and 2 dc bus capacitors. Note that this is twice as many switch pairs and dc bus capacitors, and six times as many capacitors than that required by a three level inverter. In addition, a more advanced controller is required. Because of these reasons – practicality, complexity, cost and weight - multi-level inverters with more than three levels will not be considered in this thesis.

With inverters of only three levels, many of the initial problems posed by the diode clamped inverter topology, such as maintaining intermediate dc levels, need not be solved. Since this problem is solved, and not without sacrifice, by the flying capacitor and cascaded H-bridge topologies, the above simplification greatly favors the diode clamped topology.

In addition, it was desirable to investigate multi-level topologies suitable for active front-end units in back-to-back arrangements. This is also in support of the diode clamped inverter topology.

The following chapter describes in detail the working principle and control of the diode clamped multi-level inverter topology.

3 Diode Clamped Multi-level Inverters

In this chapter, the working principle and control of the diode clamped multi-level inverter topology are explained.

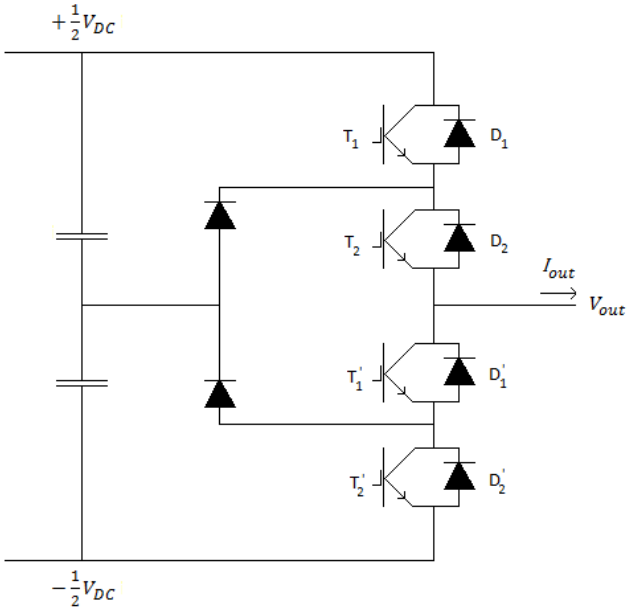

Fig 3.1 One leg of a three phase three-level diode clamped inverter

3.1 Working Principle

For a three-level diode clamped inverter, three different output voltage levels are possible, and for each either positive or negative output current is possible. Therefore there are, in total, six output voltage and current combinations.

Figure 3.2 demonstrates the fact that switches T_1 and $T_1^{'}$, figure 3.1, are complementary. That is, when T_1 is on, $T_1^{'}$ is off, and vice versa. Similarly, switches T_2 and $T_2^{'}$ are complementary. Eliminating these switch combinations, only three possible combinations are left which account for all output voltage/current states shown below.

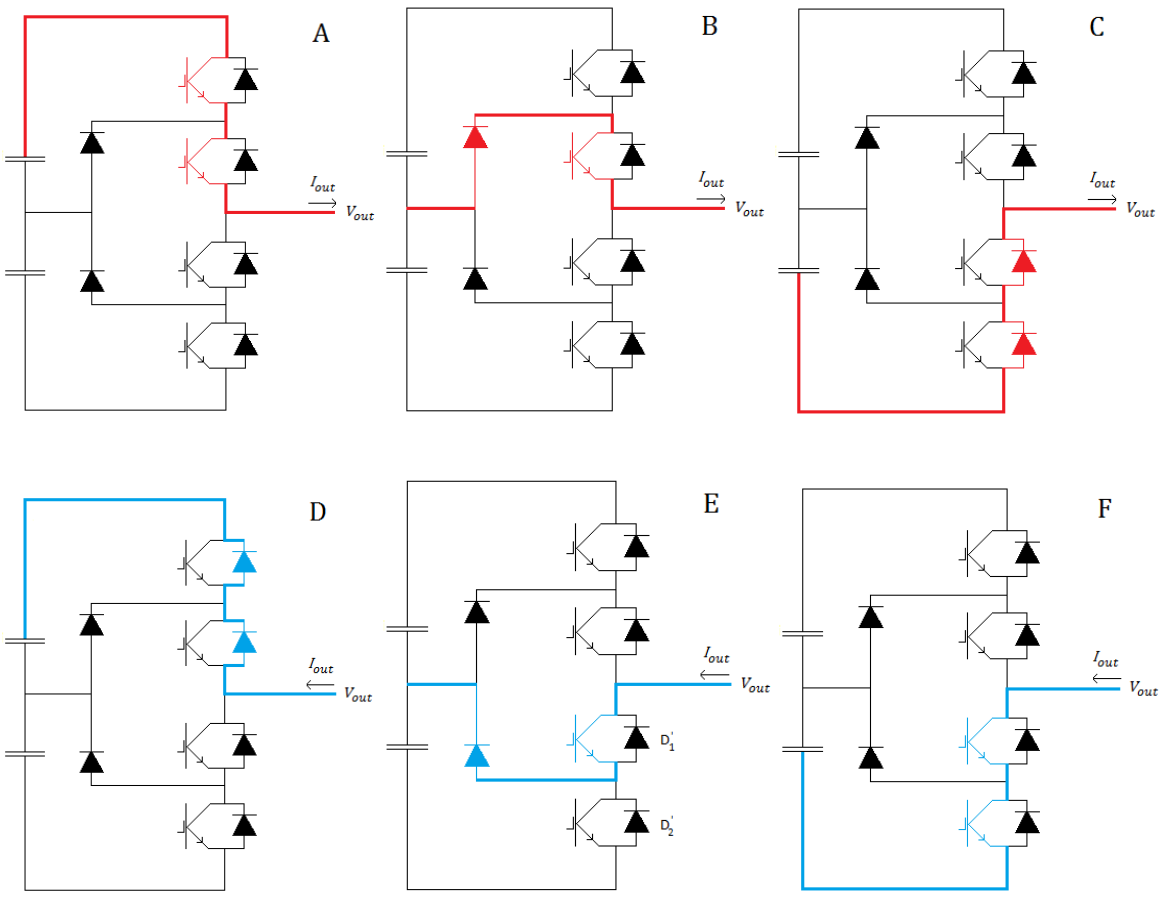

Fig 3.2 Output voltage/current combinations for three-level inverter

A. Switches T_1T_2 are on. The output voltage is $+\frac{1}{2}V_{dc}$ and output current positive, originating from the upper capacitor and reaching the output through T_1 and T_2.

B. Switches $T_2T_1^{'}$ are on. Here, the output voltage is 0. The current, which is positive, runs from the midpoint of the dc bus to the output through the upper clamp diode and collector of T_2.

C. Here, switches $T_1^{'}T_2^{'}$ are on. The output voltage is $-\frac{1}{2}V_{dc}$. Current runs from the lower capacitor, through the diodes paralleling $T_1^{'}$ and $T_2^{'}$ to the output.

D. Just as in state A, switches T_1T_2 are on. In this state, however, current runs from the output through the upper freewheeling diodes, recharging the dc bus capacitors. The output voltage is $+\frac{1}{2}V_{dc}$.

E. Switches $T_2T_1^{'}$ are on. The output voltage is, like in state B, 0. Current originating in the load runs through the collector of switch $T_1^{'}$ and the lower clamp diode to the dc bus midpoint.

F. Current originating in the load runs through switches $T_1^{'}T_2^{'}$ and reaches the bottom capacitor. The output voltage is $-\frac{1}{2}V_{dc}$.

The switch states are summarized in table 3.1 [3].

V_{out}	Switches	Path	
		$I_{out} > 0$	$I_{out} < 0$
$+{}^{1}/_{2}\,V_{dc}$	T_1T_2	A	D
0	$T_2T_1^{'}$	B	E
$-{}^{1}/_{2}\,V_{dc}$	$T_1^{'}T_2^{'}$	C	F

Table 3.1.

3.2 Modulation

In this thesis, the inverters are controlled by pulse width modulators based on the constant Volts-per-Hertz, often abbreviated VHz, principle. Pulse width modulation is explained in this section, and an explanation of the VHz principle can be found appended to the thesis.

One of the most common modulation techniques used in two-level inverters today is pulse width modulation with sinusoidal reference waveforms, often called SPWM. This technique can be extended and used in multi-level inverters.

In basic SPWM, a sine wave of desired output frequency is compared to a high frequency triangular carrier wave. If the instantaneous value of reference waveform is higher than the carrier wave, the upper transistor of the inverter phase leg is on (and the lower transistor off). Else, the lower transistor is on (and the upper transistor off).

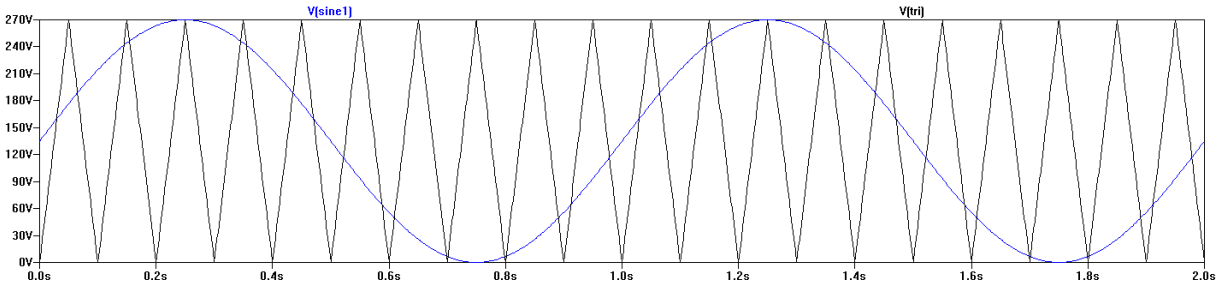

Fig 3.3 SPWM for 2-level inverter, low frequency used for clarity

Since the maximum attainable load voltage is $\frac{1}{2}V_{dc}$, the peak value of the triangular carrier wave form should also be $\frac{1}{2}V_{dc}$. The modulation index can then be defined as

$$m_a = \frac{v_{ref}}{\hat{v}_{tri}} = \frac{v_{ref}}{V_{dc}/2}$$

It is clear that overmodulation, the condition when the reference waveform exceeds the value necessary to produce maximum output, occurs for sinusoidal reference waveforms at

$v_{i,ref} = V_{dc}/2$, that is, $m_a = 1$

It is possible to achieve better dc bus utilization by using symmetrical reference waveforms. Symmetrical reference waveforms are created by calculating and subtracting a zero-sequence voltage from the sinusoidal reference waveforms [4].

$$v_{offset} = \frac{1}{2}\left(\max\left(v_{a,ref}, v_{b,ref}, v_{c,ref}\right) + \min\left(v_{a,ref}, v_{b,ref}, v_{c,ref}\right)\right)$$

$$v_{iz,ref} = v_{i,ref} - v_{offset}$$

This allows for a greater peak value of the reference waveform before overmodulation [4].

$v_{iz,ref} = \frac{V_{dc}}{\sqrt{3}}$, yielding $m_a = 1.15$

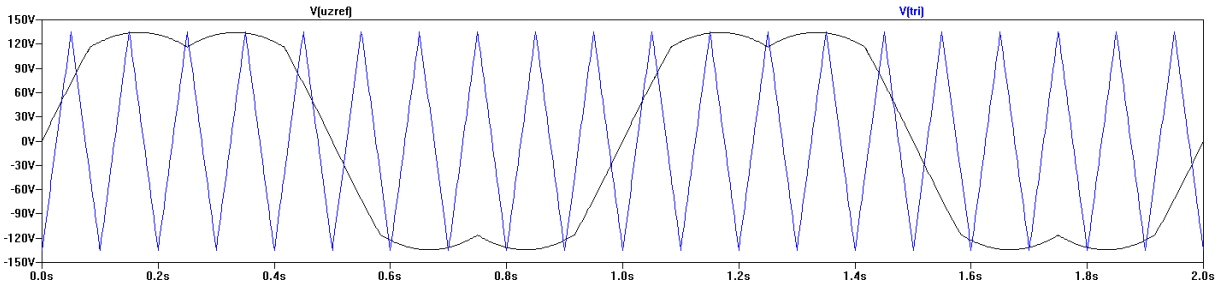

Fig 3.4 PWM with symmetrical reference waveforms for 2-level inverter

As stated above, this modulation scheme can easily be extended for use in multi-level inverters. One triangular carrier wave can be used to control two switches. Thus, for an N-level inverter, N-1 triangular carrier waves are needed.

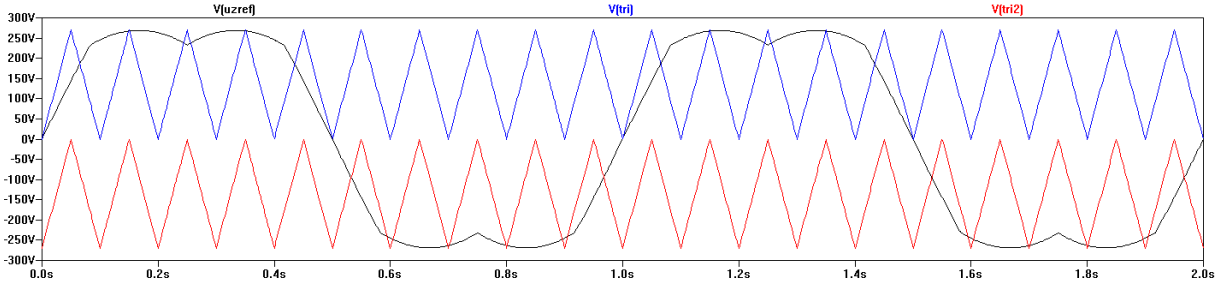

Fig 3.5 PWM with symmetrical reference waveforms for 3-level inverter

4 Simulations

In this thesis, two systems are simulated in LTspice, a freeware SPICE developed by semiconductor manufacturer Linear Technology [11]. The first system is a representation of the existing system and thus contains a three phase two-level inverter. It serves as a reference point against which all comparisons were made. The second system contains a three phase three-level diode clamped inverter and constitutes the system to be investigated. Shown below is the general structure of the investigated systems.

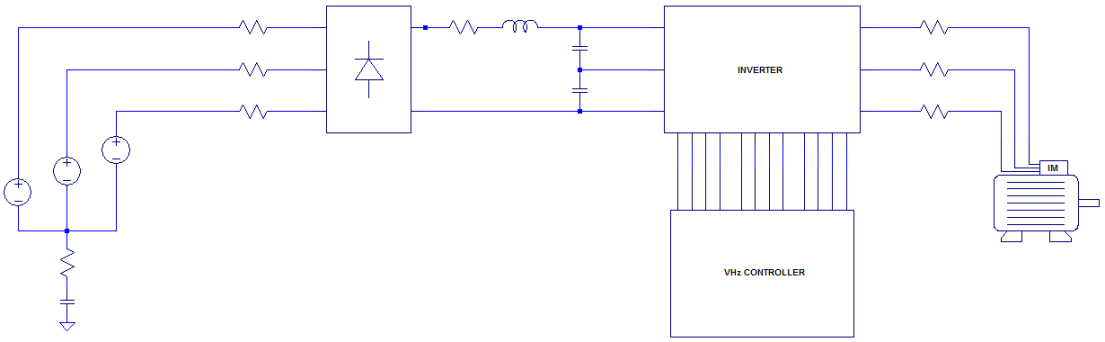

Fig 4.1 Simulation overview in LTspice

In the following section, each part of each system is explained. Then, the actual simulations are presented and the results explained.

4.1 System parts

The systems include a model of the grid, a three phase uncontrolled rectifier, an inverter with VHz controller, and an induction motor load.

4.1.1 Rectifier

The grid voltages are input to and rectified by the uncontrolled bridge. The bridge output terminals are connected to the dc bus via an intermediate inductive filter.

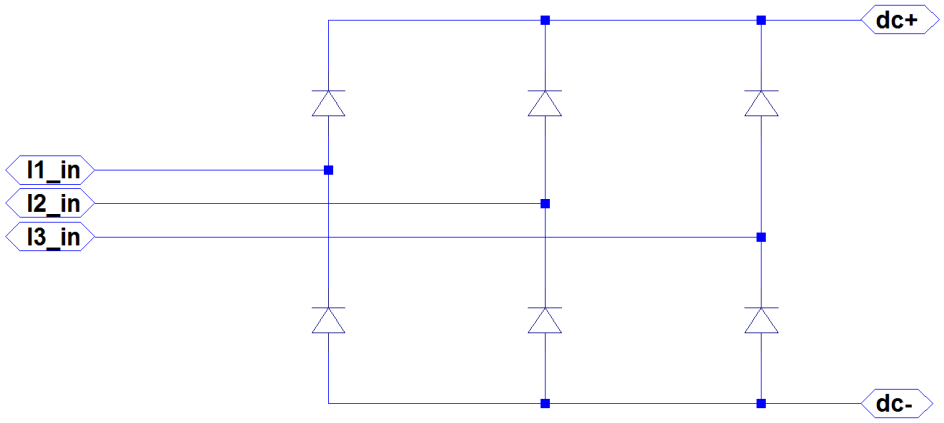

Fig 4.2 Three phase diode rectifier in LTspice

An expected value for the resulting average dc bus voltage is calculated

$$\bar{V}_{dc} = \frac{1}{T/6}\int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} V_{LL} * \cos(\omega t)\, dt$$
$$= \frac{6V_{LL}}{\omega T}\left(\sin\left(\frac{\pi}{6}\right) - \sin\left(-\frac{\pi}{6}\right)\right)$$
$$= \frac{3\sqrt{2}}{\pi} V_{LL,RMS}$$

which for $V_{LL,RMS} = 400$ gives an average dc bus voltage

$$\bar{V}_{dc} = \frac{3\sqrt{2}}{\pi} * 400 = 540V$$

This result is verified by the simulations. Shown below are the grid voltages, the rectified version (offset 50 Volts for clarity) and the resulting dc bus voltage.

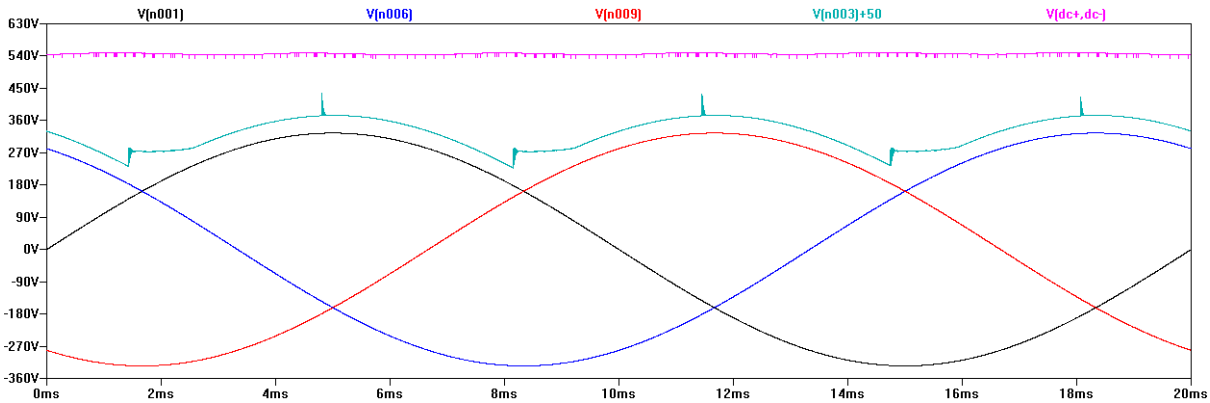

Fig 4.3 Grid voltages, rectified voltage (with offset) and dc bus voltage

The voltage across the rectifier diodes each period reaches a peak value of approximately 560V, figure 4.4.

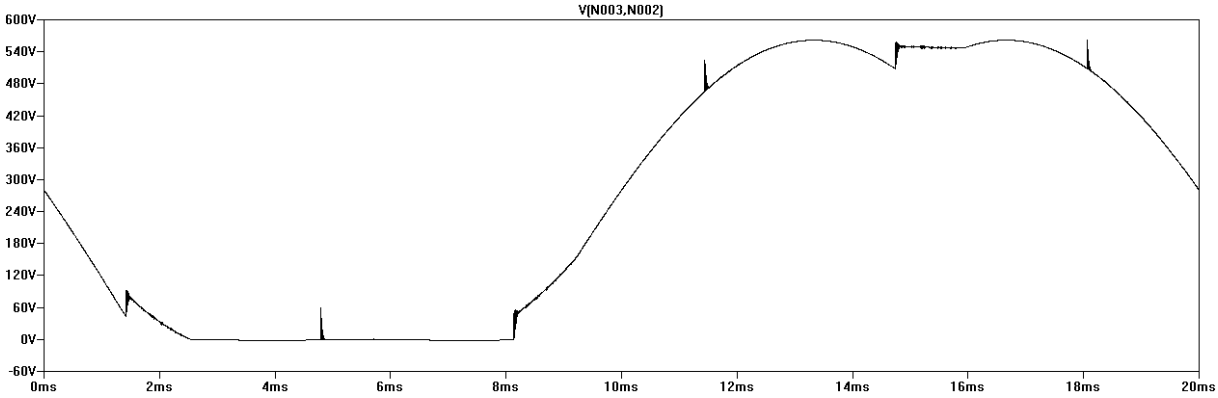

Fig 4.4. Three phase uncontrolled rectifier diode voltage

For safety reasons and practicality, d4ph50u, a diode with a voltage rating of 1200V, is chosen.

4.1.2 Inverters

The working principle of the two-level inverter circuit was briefly covered in the introductory chapter. In this section, LTspice schematics of the inverter circuit and its related driver circuit are shown.

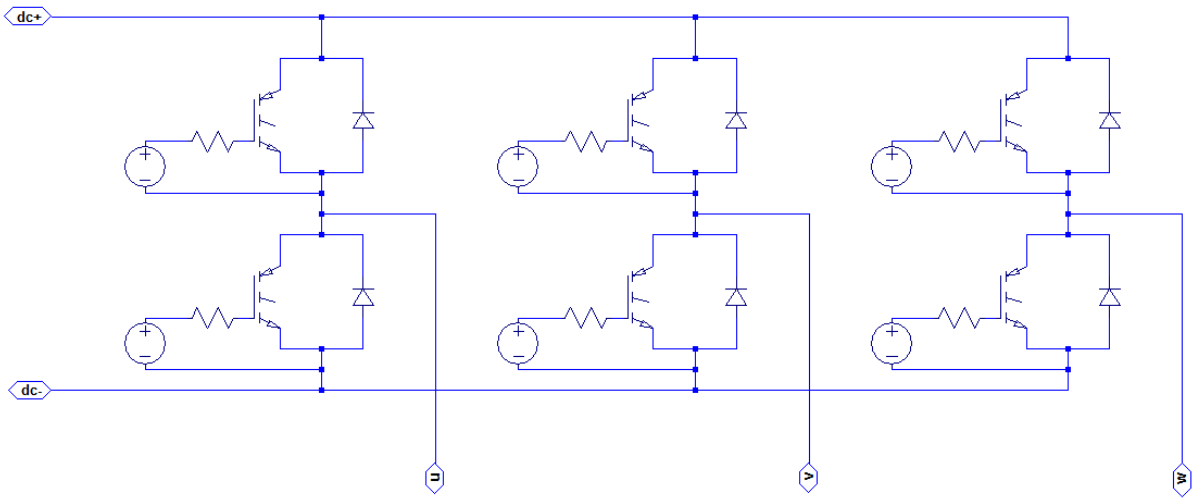

Fig 4.5 Three phase two-level inverter in LTspice

The IGBTs are controlled by a PWM modulator. A simple driver circuit is implemented by a behavioral voltage source, taking on a scaled value of the PWM signal, connecting the gate and source terminals.

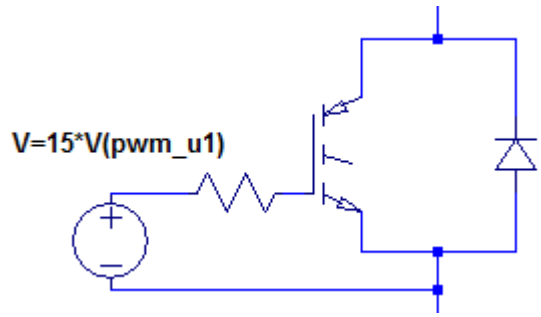

Fig 4.6 Simple IGBT driver circuit

Figure 4.7. shows that the IGBT on-state voltage is approximately 540V, that is, the dc bus voltage.

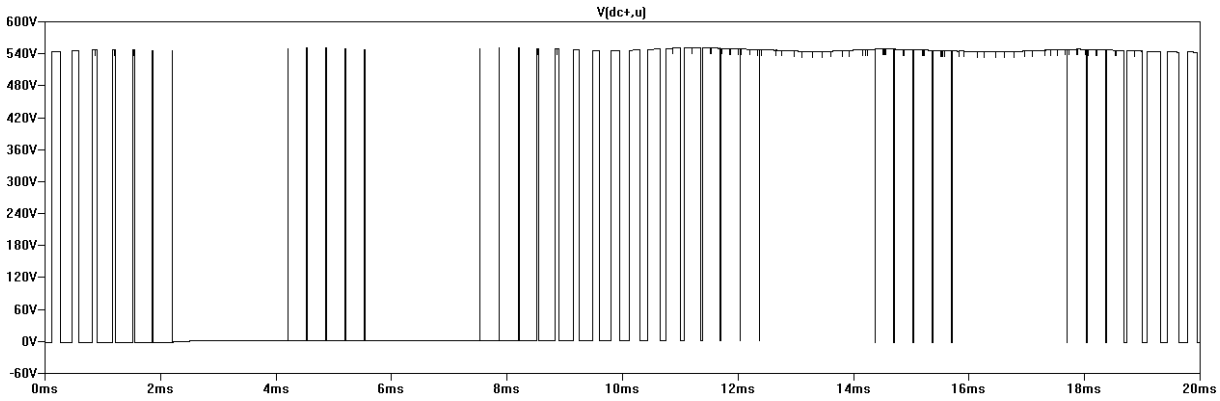

Fig 4.7 IGBT voltage for two-level inverter

Taking into account transients and possible voltage spikes, a 600V IGBT is not a safe choice and therefore a 1200V IGBT must be used.

Shown below are the three-level inverter LTspice schematics.

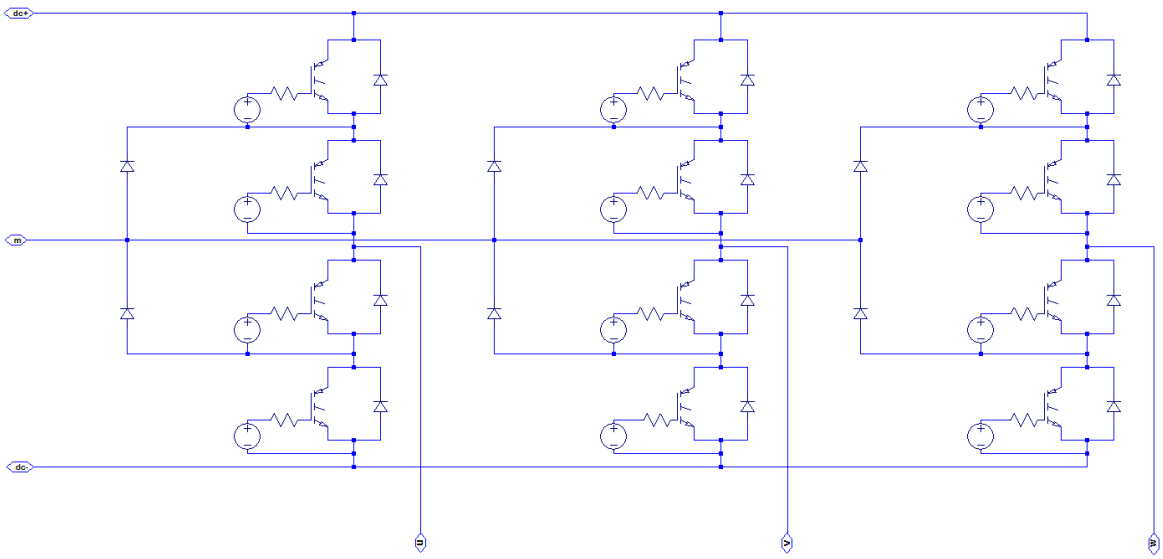

Fig 4.8 Three phase three-level inverter in LTspice

It is evident that this inverter, having more switches to control, needs a more advanced modulator than that required by a two-level inverter.

From figure 4.9, it is clear that the peak voltage is approximately 270V, half the dc bus voltage, as predicted by the theoretical model. Thus, an IGBT with lower voltage rating can be chosen.

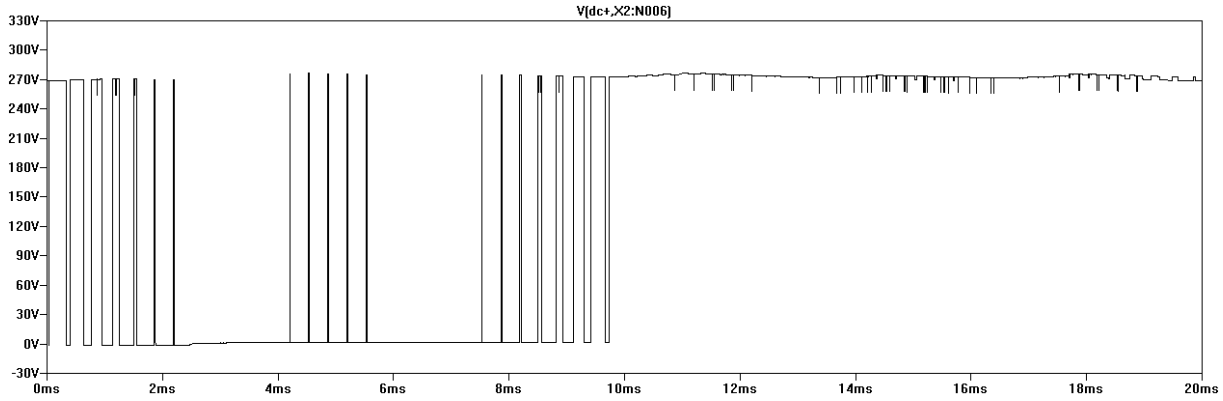

Fig 4.9 IGBT voltage for three-level inverter

It has in this section been shown that, for the two-level inverter, an IGBT with a voltage rating of 1200V must be selected and that, for the three-level inverter, an IGBT with a reduced voltage rating of 600V can be selected. The chosen IGBTs must, however, in order to conduct a fair comparison, be comparable in key aspects such as practical continuous collector current and optimum switching frequency.

Unfortunately, no 1200V IGBTs optimized for the desired switching frequency, 1-3 kHz, have accompanying SPICE models and, as a result, IGBTs optimized for switching frequencies of 8-40 kHz must be selected. Further, meeting the above constraint, only one pair of IGBTs with an approximately equal peak collector current of around 20 A has available SPICE models.

For the two-level inverter IRG4PH50U, a 1200V IGBT with accompanying anti-parallel diode D4PH50U, is selected [5].

IRG4PC40U is a 600V IGBT comparable with IRG4PH50U. It is selected for use in the three-level inverter circuit. D4PC50F is used as anti-parallel diode [6].

4.1.3 Modulators

The dc bus capacitor voltage and the desired motor speed are input to the VHz controller through sample-and-hold circuitry. The desired motor speed, n_{ref}, is used to calculate the amplitude and angular velocity of the symmetrical reference waveforms to be created.

$$V_{ref} = \left(\frac{n_{ref}}{n_{rated}}\right) V_{rated}$$

$$\omega_{ref} = \left(\frac{n_{ref}}{n_{rated}}\right) \omega_{rated}$$

Yielding

$$v_{i,ref} = \sqrt{\frac{2}{3}} V_{ref} \sin(\omega_{ref}\, t - i\frac{2\pi}{3}), \text{ for i = 0, 1, 2}$$

The symmetrical waveforms are then created, as explained in section 3.2, by the subtraction of a zero sequence component.

Note that since these waveforms are to be compared to a triangular waveform (two for the three-level inverter) having a particular relationship to the dc bus voltage, the symmetrical reference waveforms have to be scaled by the input dc bus capacitor voltage. All of this is done with behavioral voltage sources.

The final reference waveforms are then, with the help of digital circuitry, compared to the triangular carrier waves in order to create the signals controlling the IGBT inverters.

Shown below is the digital circuit used to control one phase leg of the inverter. Here, the scaled u-phase symmetrical reference waveform is compared to the triangular wave carrier in a Schmitt trigger yielding high output usable in the subsequent AND-gates if the triangular wave carrier is higher than the reference and vice versa. The buffer circuit is used for the generation of deadtime.

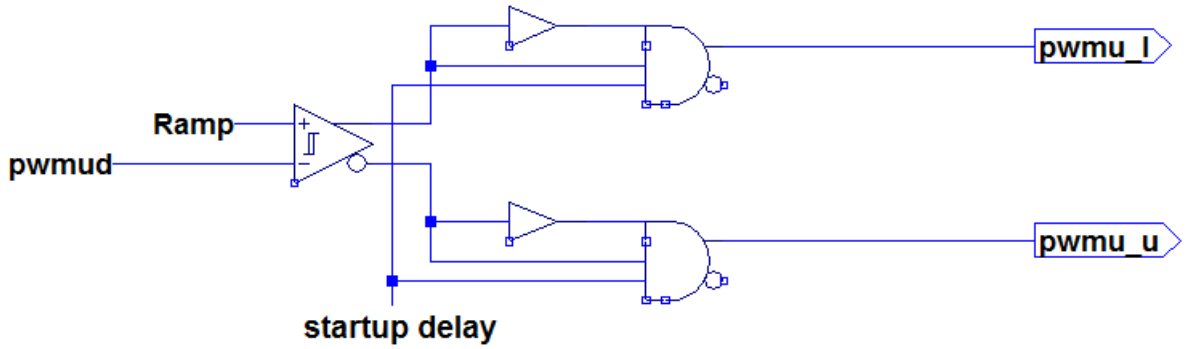

Fig 4.10 Digital circuitry used in two-level inverter modulator

As explained in section 3.2, the modulator technique can be extended for use in multi-level inverters. Extended digital circuitry is shown below.

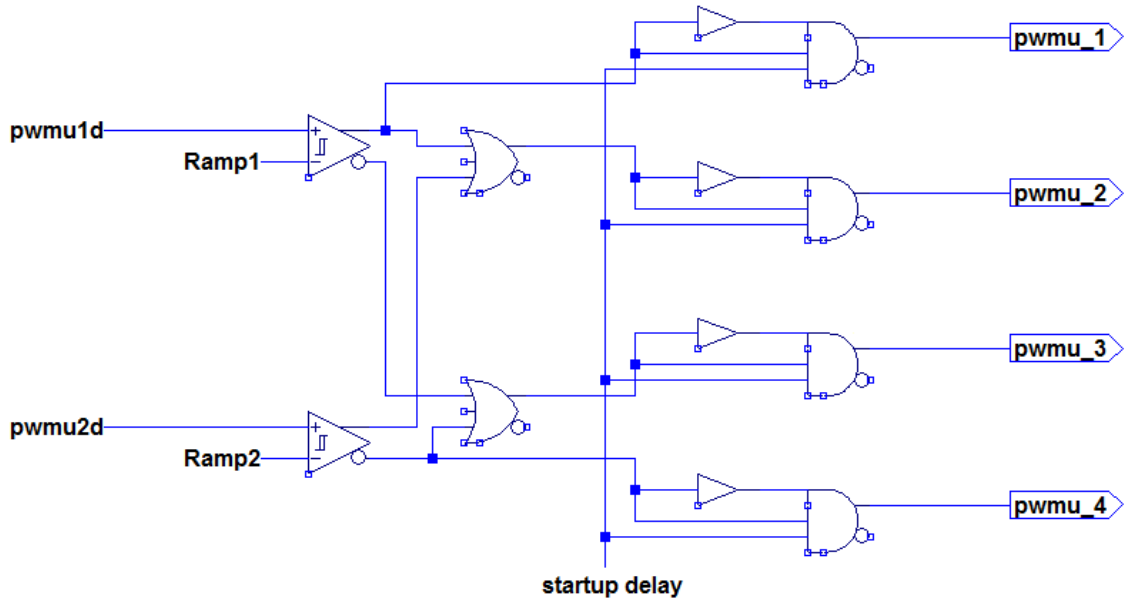

Fig 4.11 Extension of digital circuitry, for use with three-level inverters

4.1.4 Induction Motor

All simulations are made under the assumption of steady state operation. A simplified equivalent circuit is derived in appendix A, using parameters extracted from a real life machine. Below are the LTspice schematics.

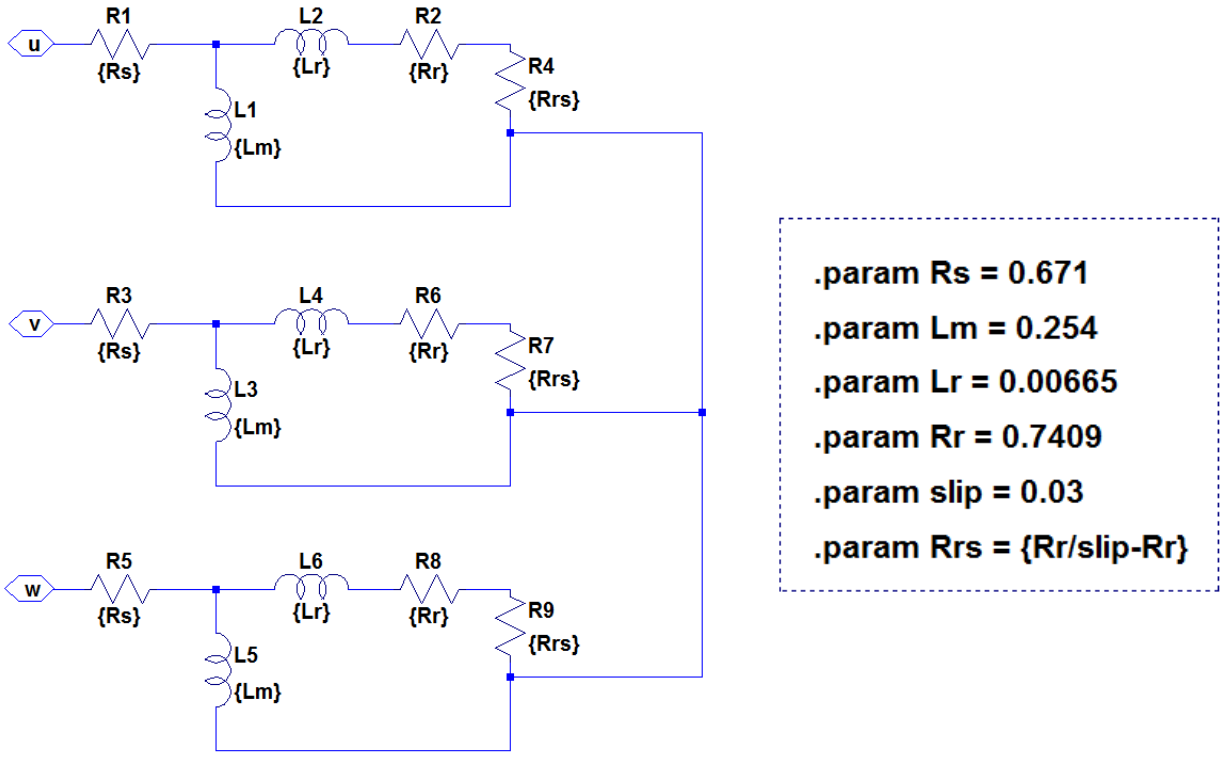

Fig 4.12 Induction motor model

4.2 SPICE model testing

Ideally, measurements made in the simulation program on the SPICE models would equal the measurements made on real life components. Generally, however, SPICE models are made for and linearised around one operating point and therefore has certain limitations regarding accuracy. As such, the SPICE models of the chosen semiconductor devices had to be validated against their corresponding datasheets. The following test circuit is implemented in LTspice.

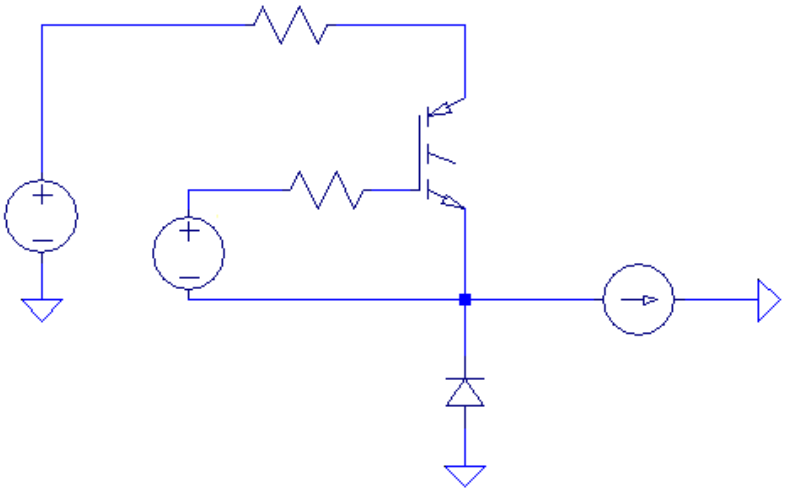

Fig 4.13 IGBT test circuit

In this circuit, current of constant magnitude must flow through either the device under test or through the diode. Measuring the collector-emitter on-state voltage allows calculation of the IGBT conduction losses.

$$P_{cond} = V_{CE,ON} * I_c * \delta$$

The energy associated with each switching action can be found through the use of an extremely low duty cycle. This value can then be used to calculate the switching losses.

$$P_{sw} = E_{TOT} * f_{sw}$$

These values can then be compared to those specified in the datasheet and eventually, if they turn out to be accurate, be used to calculate the total power dissipated in the IGBT.

$$\sum P_{loss} = V_{CE,ON} * I_c * \delta + E_{TOT} * f_{sw}$$

4.2.1 IRG4PC40U

For IRG4PC40U, the datasheet is specified for a collector current of 20 A, a collector-emitter voltage of 480V and a 10Ω gate resistor [6].

Shown below are the collector-emitter voltage and collector current for a duty cycle of 50%.

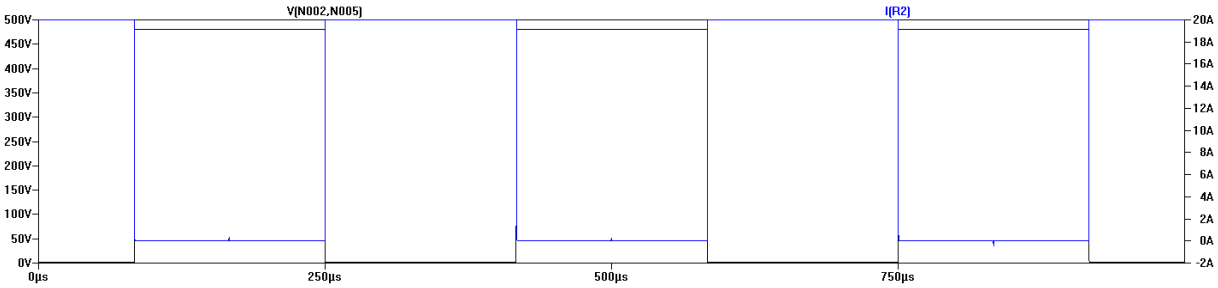

Fig 4.14 IRG4PC40U collector-emitter voltage and collector current

The collector-emitter on-state voltage are simulated to be $V_{CE,ON} = 1.9\ V$ while expecting a value of $V_{CE,ON} = 1.7\ V$ based on the information given in the datasheet. As a result, conduction losses will for this IGBT model, under these conditions, be approximately 12% higher than expected in a real life situation.

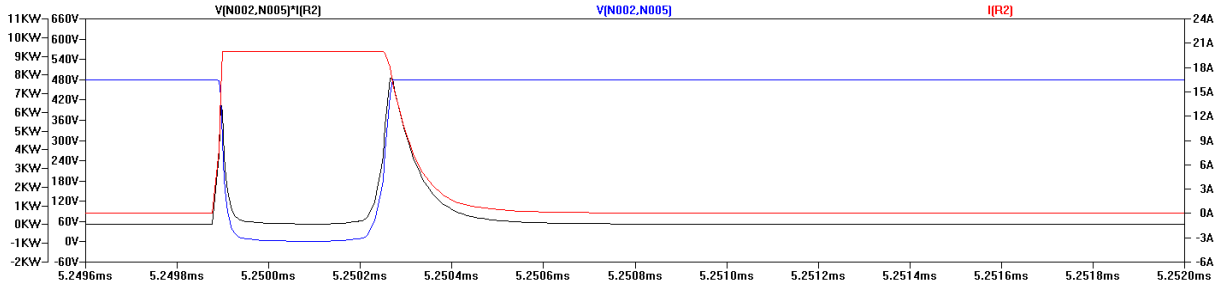

Fig 4.15 IRG4PC40U turn-on and turn-off losses

Integration of the above power waveform yields the energy associated with each turn-on and turn-off.

$$E_{TOT} = E_{on} + E_{off} = 842.73\ \mu J$$

This value is, contrary to the collector-emitter on-voltage, lower than expected and seems to coincide with the value specified for a junction temperature of 25℃ which is likely to be the temperature used for extracting model parameters for this particular device. This is not realistic and, as a result, the switching characteristics of this IGBT model are deemed inaccurate.

The total power losses are predicted and measured using $\delta = 0.3$ and $f_{sw} = 4\ kHz$ as an example.

$$\sum P_{loss} = 1.9 * 20 * 0.3 + 827.2 * 10^{-6} * 4 * 10^{3} = 14.77\ W$$

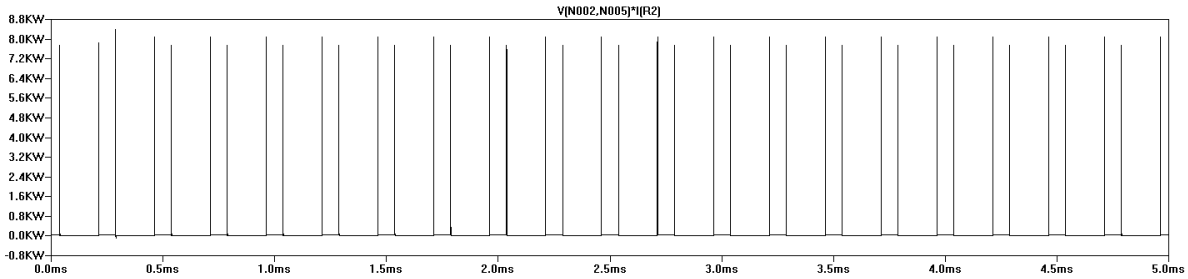

Fig 4.16 Total power loss for IRG4PC40U

The simulation yielded $\sum P_{loss} = 14.76\ W$. As such, it can be concluded that while the SPICE model very much behaves like an IGBT, it does so with inaccurate switching characteristics.

4.2.2 IRG4PH50U

The datasheet for IRG4PH50U was specified for a collector current of 24 A, a collector-emitter voltage of 960 V and a 5 Ω gate resistor. Below are the results for the simulations made under these conditions [5].

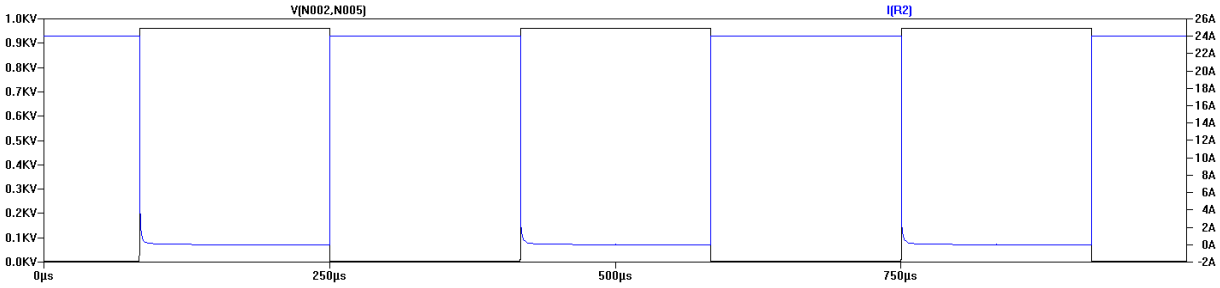

Fig 4.17 IRG4PH50U collector-emitter voltage and collector current

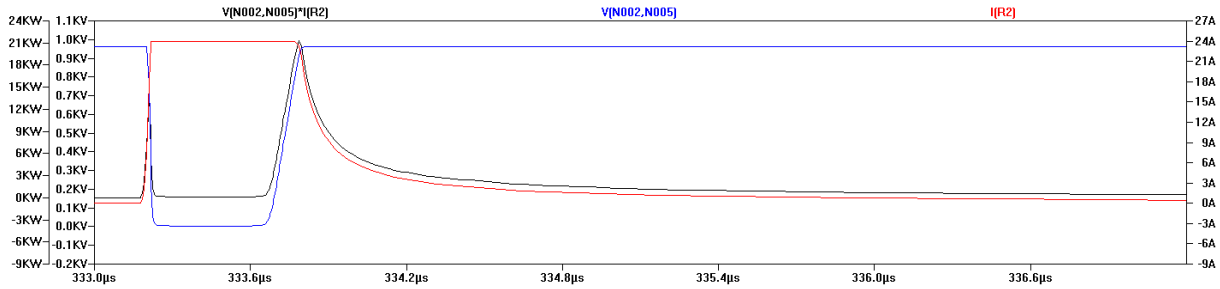

Fig 4.18 IRG4PH50U turn-on and turn-off losses

The following values are simulated.

$V_{CE,ON} = 1.95\,V$

$E_{TOT} = 7.398\,mJ$

Here, the collector-emitter on-state voltage is expected to be $V_{CE,ON} = 2.54\,V$ and, whereas the previous IGBT model, IRG4PC40U, partially matched the switching characteristics specified for an operating junction temperature of 25℃, the power losses measured for this IGBT are about twice as high as those specified for 150℃ [5].

Using, as above, $\delta = 0.3$ and $f_{sw} = 4\,kHz$ as an example, the total power losses are predicted.

$$\sum P_{loss} = 1.95 * 24 * 0.3 + 7.66 * 10^{-3} * 4 * 10^{3} = 44.68\,W$$

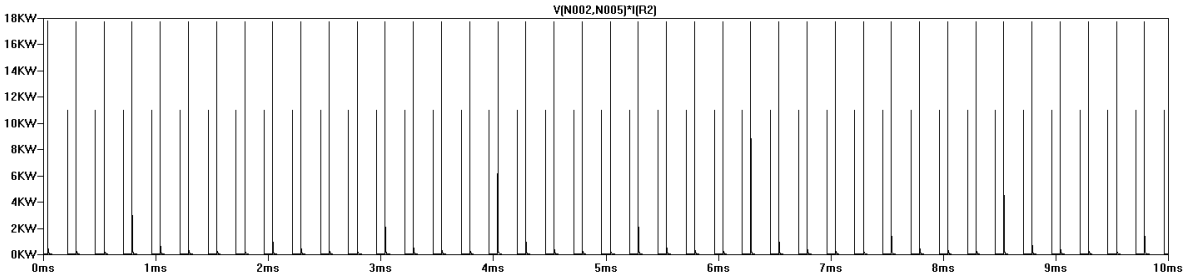

Fig 4.19 Total power loss for IRG4PH50U

This value is confirmed by the simulations, shown in fig 4.19 above. As such, it can be concluded that while the SPICE model very much behaves like an IGBT, it does so with inaccurate switching characteristics.

4.2.3 Conclusions

These simulations have shown that while the IGBT SPICE models behave very much like IGBTS, they do so with inaccurate switching characteristics. As a result, simulated values for power and hence efficiency may not be trusted. It is, however, still possible to make a comparison regarding inverter efficiency.

Comparison of conduction losses

To compare inverter conduction losses during similar conditions, both the 600V and 1200V IGBTs were simulated in the three-level inverter system.

$$\sum P_{loss} = V_{CE,ON} * I_c * \delta + E_{TOT} * f_{sw}$$

Here, both $V_{CE,ON}$ and E_{TOT} depend on the collector current. Used is a high switching frequency in the range of 15-20 kHz and, therefore, the IGBT collector current can be assumed to be equal between simulations. This assumption is justified in figures 4.20 and 4.21.

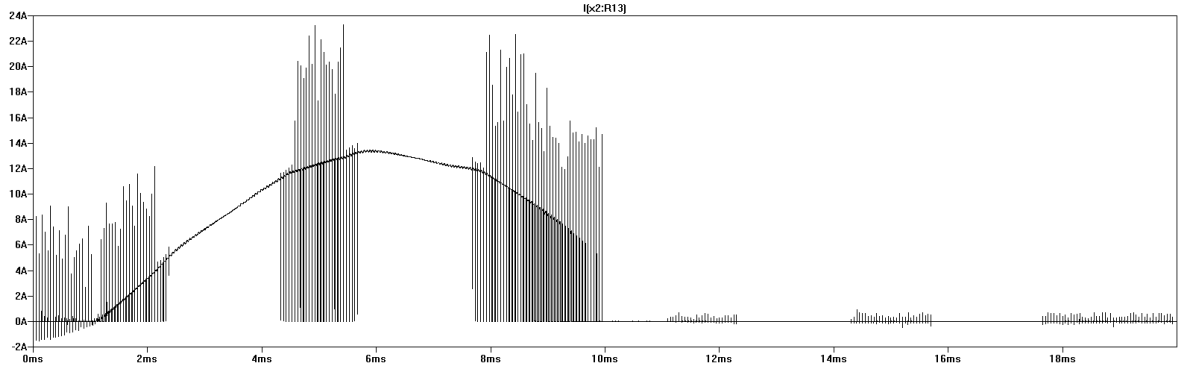

Fig 4.20 Collector current using $f_{sw} = 20000\ Hz$

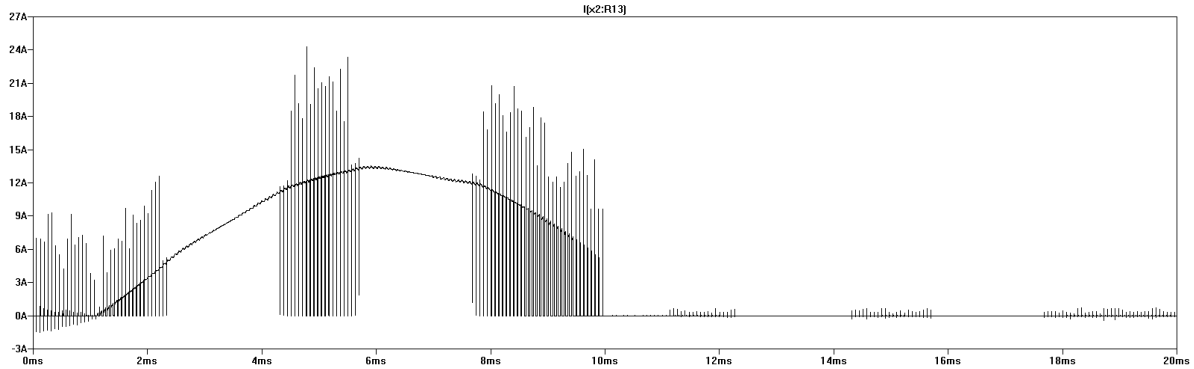

Fig 4.21 Collector current using $f_{sw} = 15000\ Hz$

It is here possible to use the results of two separate simulations to calculate an average value for the energy loss associated with each turn-on and turn-off.

$$\bar{E}_{TOT} = \frac{\sum P_2 - \sum P_1}{f_2 - f_1}$$

This value can in turn be used to separate the conduction losses from the switching losses.

$$P_{cond} = \sum P_{loss} - \bar{E}_{TOT} * f_{sw}$$

The following values are simulated for the uppermost IGBT of the three-level inverter.

$P_{cond\ ,3,1200} = 11.863\ W$

$P_{cond\ ,3,600} = 6.226\ W$

These values are then, by calculating the duty cycles of the respective IGBTs, used as a basis for comparison.

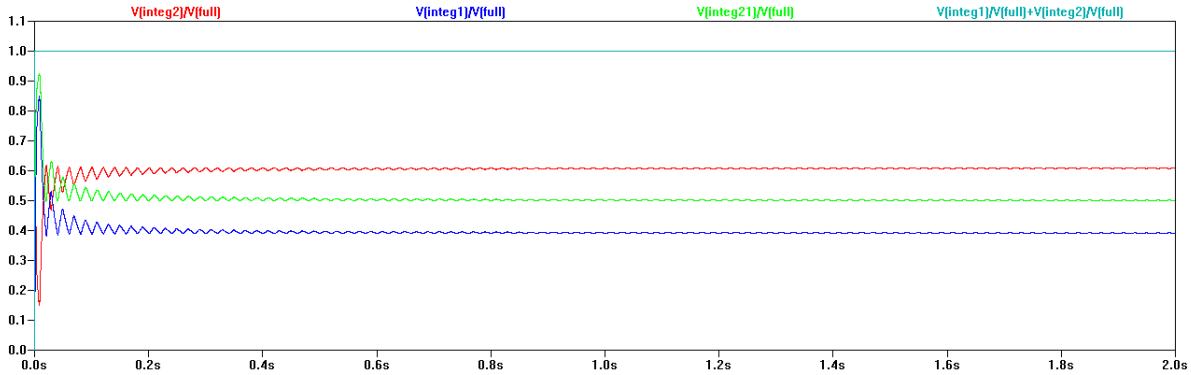

Fig 4.22 IGBT duty cycles

As stated above, all calculations were made on the uppermost IGBT of the three-level inverter. It is seen in fig 4.22 that this IGBT has a duty cycle (shown in blue) converging towards 0.4. As such, the conduction losses of the uppermost IGBT in the two-level inverter, having a duty cycle (shown in green) converging towards 0.5, will be slightly higher than those simulated above.

The losses of the two uppermost IGBTs in the three-level inverter are calculated as

$$P_{cond\ ,3} = V_{CE,ON,1} * I_{C,1} * \delta_1 + V_{CE,ON,2} * I_{C,2} * \delta_2$$

Assuming the average and RMS values of $I_{C,1}$ and $I_{C,2}$ to be equal, this expression takes the form

$$P_{cond\ ,3} = V_{CE,ON} * I_C * (\delta_1 + \delta_2)$$

Since the sum of the duty cycles is approximately twice of that used for the calculations above, the conduction losses will also be approximately twice the value of that calculated above. It is also seen that this value nearly equals the value calculated for the two-level inverter. As a result, it is possible make a comparison regarding efficiency based entirely on switching losses.

It should here be pointed out that, in reality, the conduction losses are expected to be in favor of the three-level inverter. This is partially due to a higher than expected on-state voltage for the 600V IGBT, and a lower than expected on-state voltage for the 1200V IGBT. In addition, it was for simplicity assumed that $I_{C,1}$ was equal to $I_{C,2}$ when, in reality, $I_{C,1}$ is smaller.

Comparison of switching losses

Switching losses are proportional to the switching frequency and also have an almost linear relationship with collector current and collector-emitter voltage. Using datasheet specifics, one can find the following relationship [5, 6]

$$\frac{E_{TOT,3}}{E_{TOT,2}} \approx {}^{1}/_{3}$$

Yielding the following expression

$$\frac{\sum P_{sw,3}}{\sum P_{sw,2}} = \frac{2 * E_{TOT,3} * f_{sw,3}}{E_{TOT,2} * f_{sw,2}} = {}^{2}/_{3} * \frac{f_{sw,3}}{f_{sw,2}} = \{f_{sw,3} = f_{sw,2}\} = {}^{2}/_{3}$$

As such, the three-level inverter, using the same switching frequency as the two-level inverter, is expected to outperform the two-level inverter concerning both efficiency and power quality.

It is here possible to first establish a baseline THD using the two-level inverter system and then, in the three-level inverter system, by reducing switching frequency, aim for the same THD, yielding an increase in inverter efficiency. It is also possible to instead use the two-level inverter efficiency as a baseline and increase switching frequency, yielding an increase in THD. These possibilities are explored further in the subsequent sections.

4.3 Simulations

As previously discussed, the main objective of this thesis is to evaluate the advantages and drawbacks of the diode clamped multi-level inverter topology in terms of efficiency, power quality, cost, weight and complexity.

The purpose of this part of the thesis, which presents the inverter system simulation results, is to get an understanding of the situation regarding efficiency and power quality.

Efficiency will be calculated by simulating inverter input power and power losses in IGBTs and diodes

$$\eta = \frac{P_{in} - P_{loss}}{P_{in}}$$

The quantity chosen for power quality is the total harmonic distortion in the stator current, defined as

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty}(I_{RMS,h})}}{I_{RMS,1}} = \frac{\sqrt{I_{RMS}^2 - I_{RMS,1}^2}}{I_{RMS,1}}$$

Furthermore, all simulations are done under the assumption of steady state operation. Thus, at the beginning of each simulation, the capacitors are already precharged and the motor is assumed to be running.

First, the two-level inverter system will be simulated in order to establish a baseline against which the simulation results of the three-level inverter system can be compared.

4.3.1 Simulations of the two-level inverter system

Shown below is the output current of one of the phases. Clearly, the peak value of the output current is lower than the current rating of the IGBT.

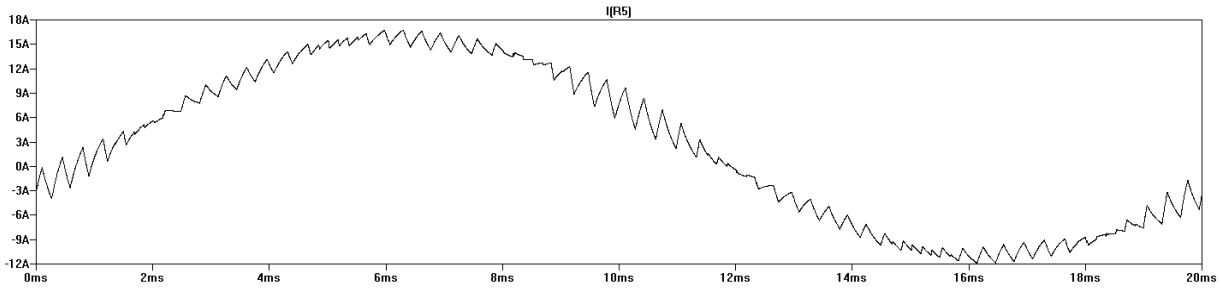

Fig 4.23 Output current using $f_{sw} = 3000$ Hz

As stated above, the quantity chosen for power quality is the total harmonic distortion, defined as

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty}(I_{RMS,h})}}{I_{RMS,1}} = \frac{\sqrt{I_{RMS}^2 - I_{RMS,1}^2}}{I_{RMS,1}}$$

The RMS value of the current is calculated by a behavioral voltage source in LTspice as

$$I_{RMS} = \sqrt{\frac{1}{T}\int (i(t))^2\, dt} = 9.516\, A$$

The fundamental component of the current can then be extracted from its harmonic spectrum.

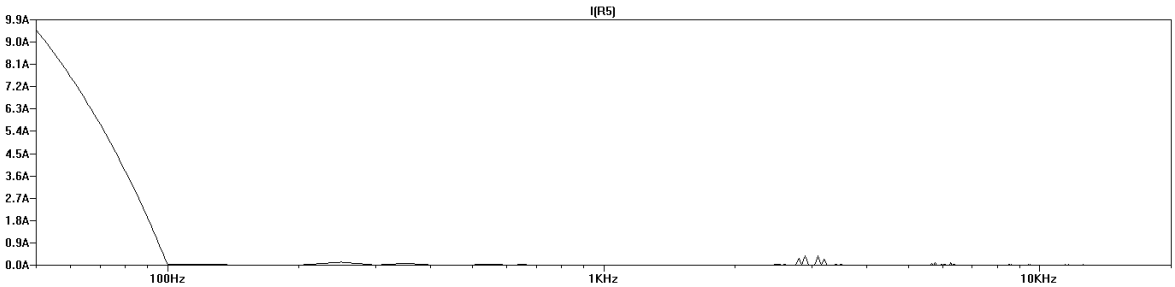

Fig 4.24 Harmonic spectrum of output current using $f_{sw} = 3000$ Hz

$I_{RMS,1} = 9.4894\, A$

This now allows for a calculation of the total harmonic distortion

$$THD = \frac{\sqrt{9.516^2 - 9.4894^2}}{9.4894} = 7.49\ \%$$

This value will serve as a baseline for subsequent simulations. Shown below are the power input to the inverter and the power dissipated in the inverter.

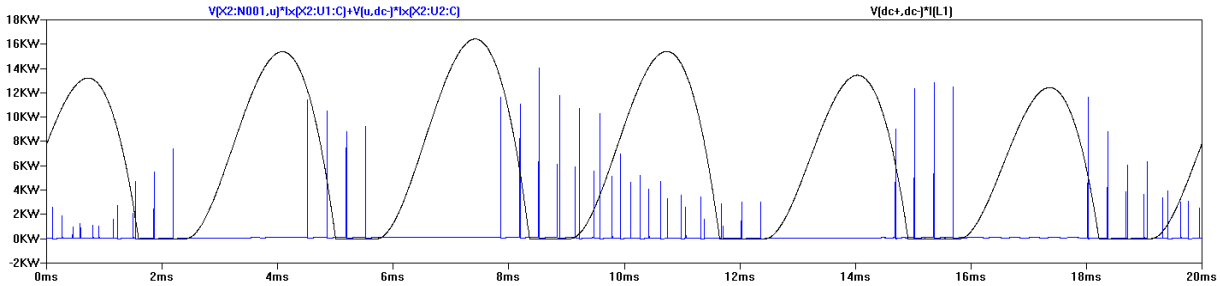

Fig 4.25 Input power and dissipated power using $f_{sw} = 3000$ Hz

The values for average power are calculated with the use of behavioral voltage sources and are shown to be

$$\bar{P}_{in} = 6.217\ kW$$

$$\bar{P}_{loss} = 3 * 76.98\ W = 230.94\ W$$

Yielding an efficiency of

$$\eta = \frac{6.217 * 10^3 - 230.94}{6.217 * 10^3} = 96.3\ \%$$

Taking into account the fact that in reality lower switching losses, as shown in the previous section, would be attained as well as the fact that an IGBT optimized for a lower switching frequency would be used, thereby reducing conduction losses, a higher real-life efficiency is to be expected.

4.3.2 Simulations of the three-level inverter system

Shown below is the output current for one of the phases in the three-level inverter system. The peak value of this current is well under the rated current of the IGBT. It is also immediately seen that this current is smoother than the one produced by the two-level inverter.

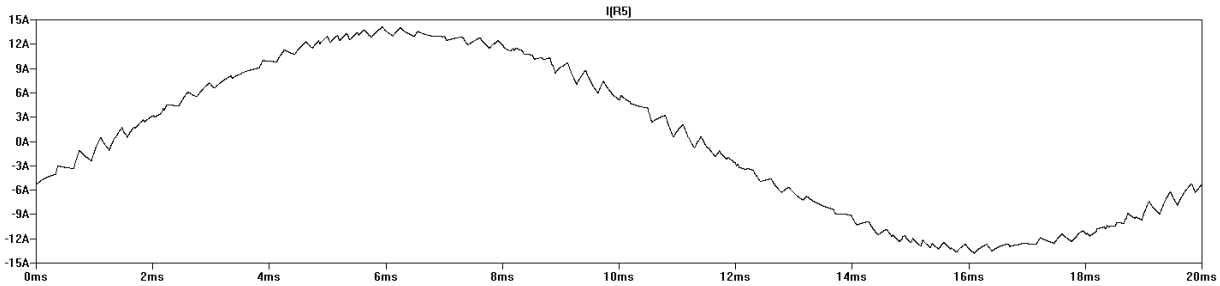

Fig 4.26 Output current using $f_{sw} = 3000$ Hz

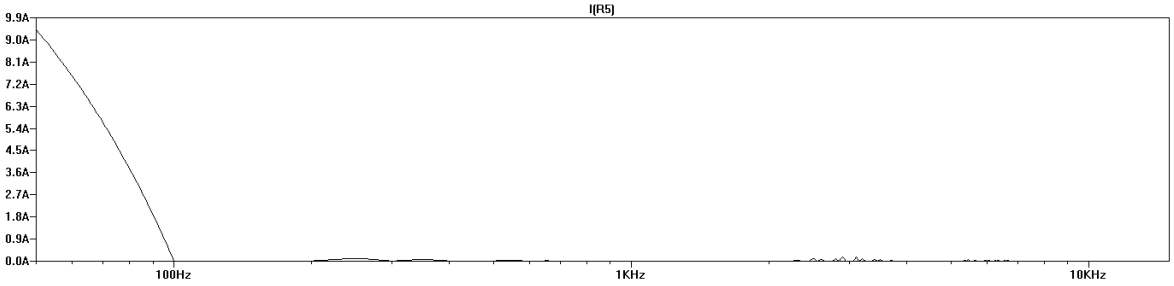

Fig 4.27 Harmonic spectrum of output current using $f_{sw} = 3000$ Hz

The RMS values of the output current and its fundamental component were, following the above outlined procedure, calculated

$$I_{RMS} = \sqrt{\frac{1}{T}\int (i(t))^2\, dt} = 9.4120\ A$$

$$I_{RMS,1} = 9.4045\ A$$

These calculations verify that the quality of the output current produced by the three-level inverter is indeed better than that of the two-level inverter.

$$THD = \frac{\sqrt{9.4120^2 - 9.4045^2}}{9.4045} = 3.983\%$$

Shown below are the power input to the inverter and the power dissipated in the inverter.

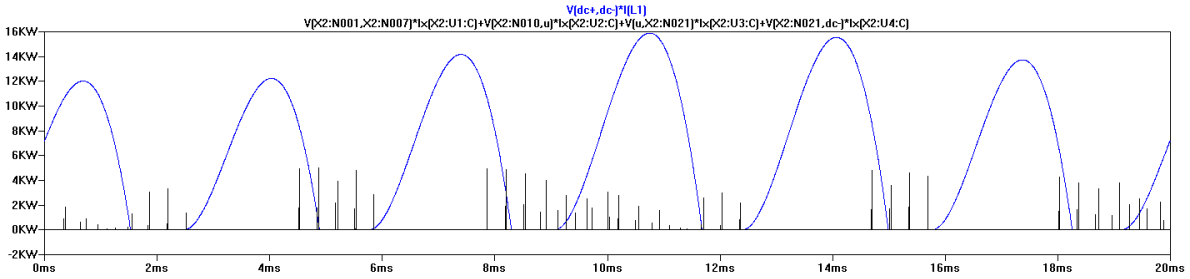

Fig 4.28 Three-level inverter input and dissipated power using $f_{sw} = 3000$ Hz

$\bar{P}_{in} = 5.9622\ kW$

$\bar{P}_{loss} = 3 * 25.972\ W = 77.916\ W$

$$\eta = \frac{5.9622 * 10^3 - 77.916}{5.9622 * 10^3} = 98.69\ \%$$

It is seen that both better efficiency and total harmonic distortion compared to that of the two-level inverter have been achieved. Below, the switching frequency will first be decreased, in order to further increase efficiency.

The switching frequency of the three-level inverter transistors is reduced until a THD approximating that of the two-level inverter system is attained. Shown below are the output current and corresponding harmonic spectrum after the switching frequency is halved.

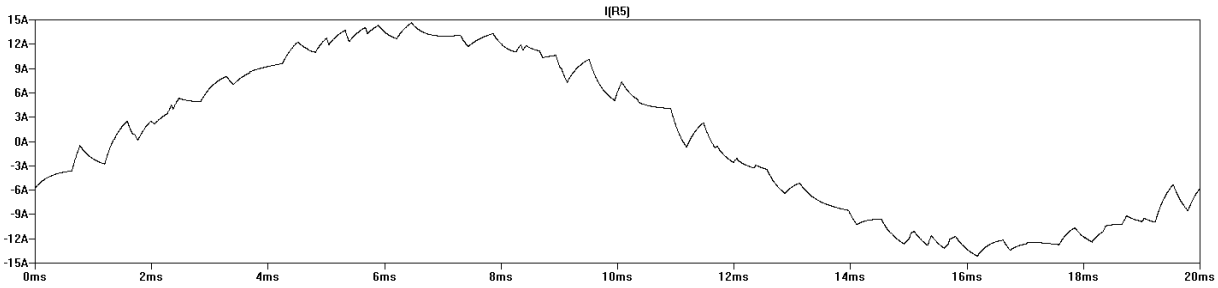

Fig 4.29 Output current using $f_{sw} = 1500$ Hz

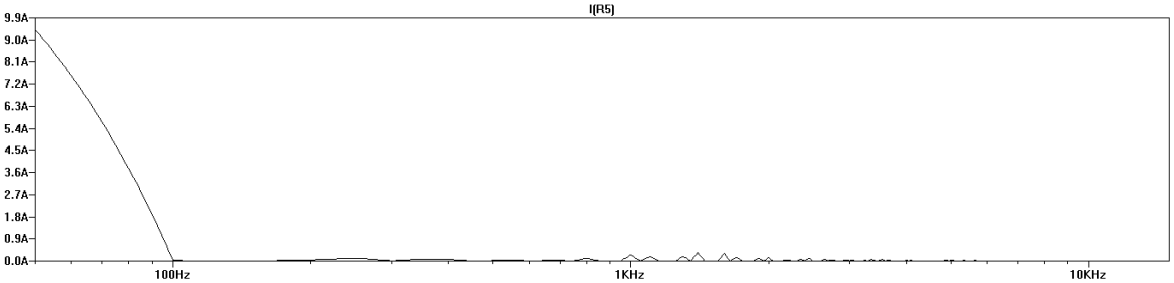

Fig 4.30 Harmonic spectrum for output current using $f_{sw} = 1500$ Hz

$$I_{RMS} = \sqrt{\frac{1}{T}\int (i(t))^2\ dt} = 9.444\ A$$

$I_{RMS,1} = 9.419\ A$

$$THD = \frac{\sqrt{9.444^2 - 9.419^2}}{9.419} = 7.29\ \%$$

This value for total harmonic distortion approximates that of the two-level inverter and, as a result, since the switching frequency was halved, switching losses have been halved.

Shown below are the input power and dissipated power using halved switching frequency.

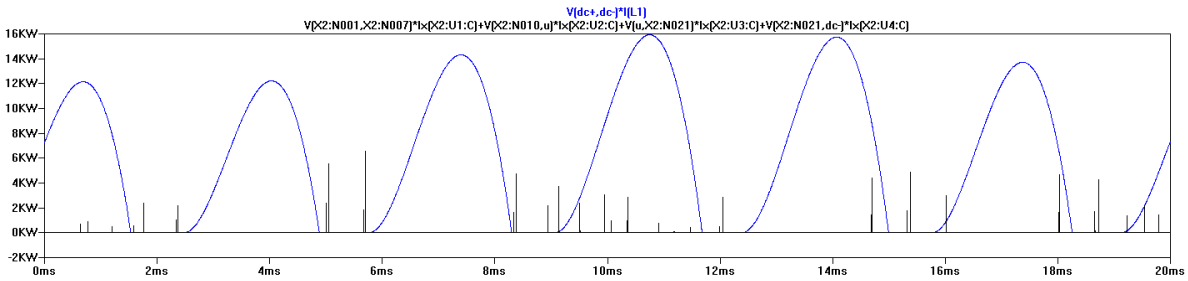

Fig 4.31 Three-level inverter input and dissipated power using $f_{sw} = 1500$ Hz

$\bar{P}_{in} = 6\ kW$

$\bar{P}_{loss} = 3 * 25.956\ W = 77.868\ W$

$$\eta = \frac{6 * 10^3 - 77.868}{6 * 10^3} = 98.7\ \%$$

It is seen that the increase in efficiency is insignificant.

Integrating the power of the uppermost IGBT shows that each switching action, shown as spikes in fig 4.32, contribute very little to the total losses.

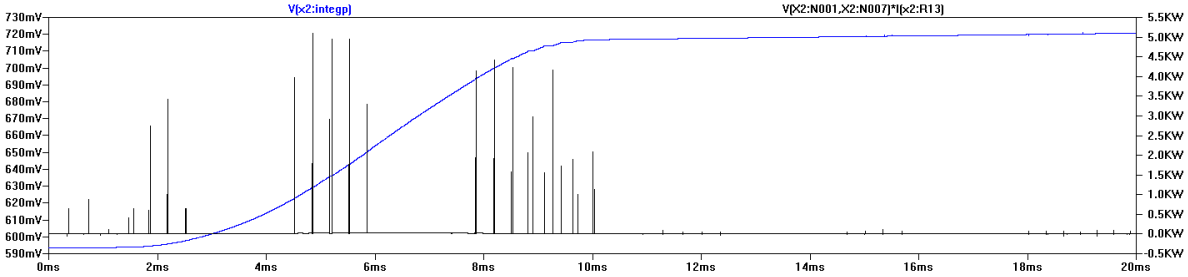

Fig 4.32 Integration of dissipated power

This is explained by the fact that the IGBTs used in these simulations have been optimized for switching frequencies between 8-40 kHz. This means that the manufacturer, expecting a high operating frequency, has aimed for lower switching losses at the expense of conduction losses. In this thesis, however, a relatively low operating frequency of only 3 kHz is used and, as a result, switching losses account for only a fraction of the total losses.

Above, the switching frequency was decreased in order to decrease switching losses. Now, the switching frequency is increased to improve the total harmonic distortion.

The switching loss comparison expression, repeated below, suggests that an increase in THD is possible at the cost of increased switching losses.

$$\frac{\sum P_{sw,3}}{\sum P_{sw,2}} = {}^{2}/_{3} * \frac{f_{sw,3}}{f_{sw,2}}$$

In the following simulation, equal switching losses were aimed for and thus the switching frequency increased by a factor $3/2$. The simulation results are shown below.

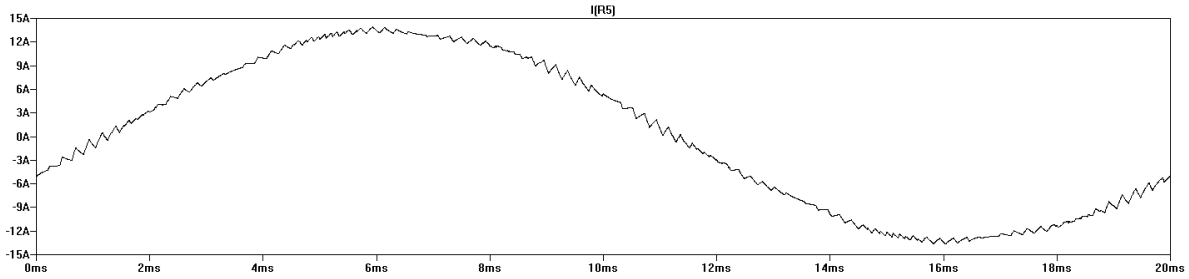

Fig 4.33 Output current using $f_{sw} = 4500$ Hz

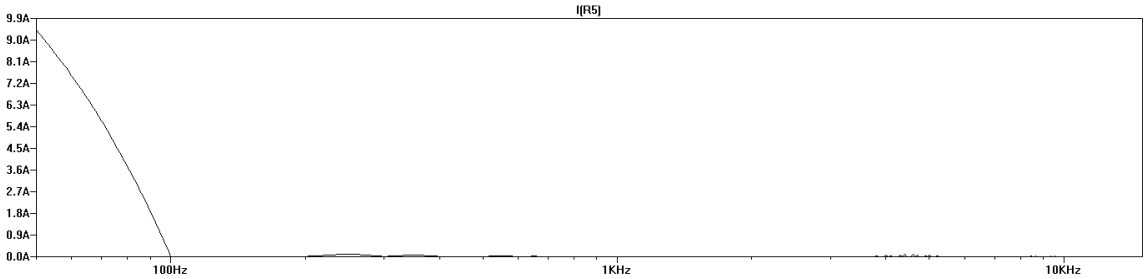

Fig 4.34 Harmonic spectrum of output current using $f_{sw} = 4500$ Hz

$$I_{RMS} = \sqrt{\frac{1}{T}\int (i(t))^2 \, dt} = 9.4059 \, A$$

$$I_{RMS,1} = 9.4045 \, A$$

$$THD = \frac{\sqrt{9.4059^2 - 9.4045^2}}{9.4045} = 1.71\%$$

This value for total harmonic distortion is almost four and a half times lower than that simulated with the two-level inverter. This improvement, as

suggested in the introductory chapter, may prove very advantageous in active front-end configurations. This is explained further in the forthcoming chapter.

The efficiency was, as expected due to above reasoning, practically static.

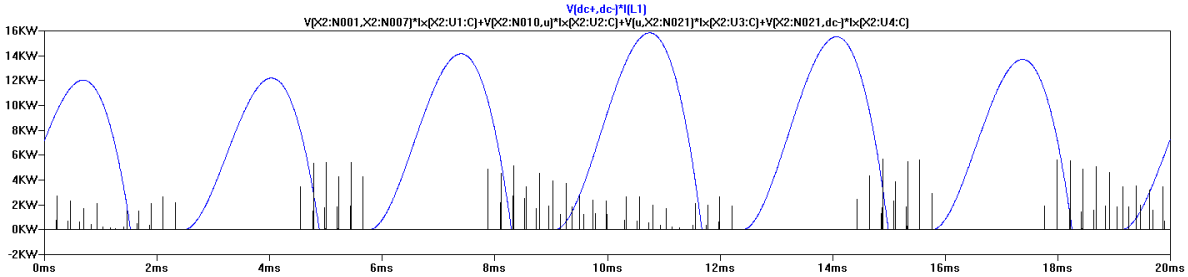

Fig 4.35 Input/dissipated power for $f_{sw} = 4500$ Hz

$\bar{P}_{in} = 5.95\ kW$

$\bar{P}_{loss} = 3 * 26.064\ W = 78.192\ W$

$$\eta = \frac{5.95 * 10^3 - 78.192}{5.95 * 10^3} = 98.68\ \%$$

5 Inverter Comparisons

It has been shown that, using the standard switching frequency of 3 kHz, the three-level inverter outperforms the two-level inverter regarding both efficiency and total harmonic distortion. It has also been shown that it is possible, by altering the switching frequency, to improve further either the efficiency or the total harmonic distortion.

This flexibility, however, is at the cost of requiring additional semiconductor devices and a more advanced modulator. This chapter provides a comparison by taking into account the results of the previous chapter as well as determinants such as cost, weight and space requirements.

Note that it is very difficult to make a true comparison seeing that, in reality, one must consider quantities to purchase, availability, discounts and more. As a result, in order to have a basis for comparison, all pricing information will be taken from the manufacturer website [7] with the assumption that only one inverter will be built and that no discounts are applicable.

Two-level inverter

As shown in fig 4.5, the two-level inverter requires six IGBTs and accompanying diodes. The IGBT used in the two-level inverter, IRG4PH50U, is available with anti-parallel diode at the cost of $6.828, yielding a total inverter cost of $6.828 * 6 \approx \$41$.

The weight of the components (IGBT and diode) is 6 grams, giving a total weight of 36 grams.

Three-level inverter

The three-level inverter, shown in fig 4.8, requires twelve IGBTs and accompanying diodes.IRG4PC40U is available with accompanying diode at the cost of $4.3, yielding a total inverter cost of $4.3 * 12 \approx \$52$.

The weight of the components is also 6 grams, giving a total weight of 72 grams.

Comparison

As expected, the three-level inverter, requiring more semiconductor devices, is more expensive than the two-level inverter. Note, however, that the semiconductor devices used in the above calculations and the conditions posed for the comparison are unrealistic. Performing the above calculations using pricing and quantities obtained at CG Drives & Automation yields a relationship showing, taking into account only the cost of the semiconductor devices, that the three-level inverter will be approximately 60% more expensive than the two-level inverter [8].

It is also of importance to consider the practical modulator differences. Concentration has in this thesis been on the purely theoretical aspects of inverter modulators and they were in all simulations largely emulated by behavioral voltage sources. In practice, however, additional hardware will be required to extend the principle to work with multi-level inverters.

Additional costs will, of course, also come in the form of the work required to develop working and practical modulator and inverter circuits.

While differences in weight and space requirements regarding the actual inverter have been shown to negligibly small, it is with the three-level inverter possible to increase switching frequency while attaining, as compared to the two-level inverter, equal efficiency in order to improve total harmonic distortion. This, as has been suggested, may be very interesting when used in active front-end configurations.

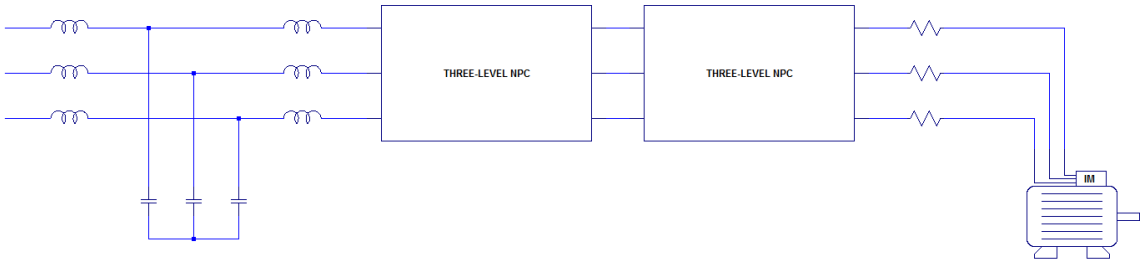

Fig 5.1 Active Front-End Configuration with L-C-L filter

In such a set-up, an L-C-L filter is necessary in order to decrease the total harmonic distortion. This filter is in practice very cumbersome, and it would therefore be very interesting if, by replacing the inverter, the THD could be decreased enough to use a reduced filter. This may in turn prove to be very advantageous regarding both cost, weight and space requirements.

6 Conclusions

This thesis investigates the viability of multi-level inverter topologies as a way to improve efficiency and power quality. For the conditions specified, the diode clamped multi-level inverter topology is found to be best suited and selected for further investigation.

The SPICE models selected and used to build the inverter circuits are shown to be inaccurate and therefore not trustworthy. A method to estimate inverter efficiency using datasheets is presented and used to show that the multi-level inverter outperforms the two-level inverter regarding both efficiency and power quality.

The estimation method is further used to calculate a specific interval in which switching frequency can be altered. Decreasing the switching frequency yields a further increase in efficiency while increasing the switching frequency betters the total harmonic distortion and hence power quality. It is also shown that improved power quality may be very attractive for active front-end units. Hence, the simulations conclusively confirm the advantages proposed in the introductory chapter.

The drawbacks of multi-level inverter topologies are also confirmed and somewhat quantified through calculations using values from the manufacturer website.

It is, however, using the results of this thesis only, impossible to conclude whether or not the use of multi-level inverter topologies will be a worthwhile pursuit. Each application has its specific needs and requirements and only through separate simulations and practical tests will it be possible to determine the status of the multi-level inverter as compared to the already existing two-level inverter.

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Appendix A - Nomenclature

Abbreviations

AC	Alternating current
DC	Direct current
EMDS	Electric motor driven systems
IGBT	Insulated gate bipolar transistor
NPC	Neutral point clamp
PWM	Pulse width modulation
RMS	Root mean square
SPICE	Simulation program with integrated circuit emphasis
THD	Total harmonic distortion
VHz	Volts per hertz
VSD	Variable speed drive
VSI	Voltage source inverter

Symbols

B_{rated}	Rated value of motor flux density
E_{off}	Energy associated with IGBT turn-off
E_{on}	Energy associated with IGBT turn-on
E_{tot}	$E_{on} + E_{off}$
$I_{RMS,1}$	RMS value of current fundamental
I_{RMS}	RMS value of current
I_c	IGBT collector current
I_{out}	Output current
L_m	Magnetizing inductance
L_r	Rotor inductance
P_{cond}	IGBT conduction losses
P_{in}	Inverter input power
P_{loss}	Inverter losses
P_{sw}	IGBT switching losses
R_r	Rotor resistance
R_s	Stator resistance
$V_{CE,ON}$	V_{CE} when IGBT is conducting
V_{CE}	Collector-emitter voltage of IGBT
$V_{LL,RMS}$	RMS value of V_{LL}
V_{LL}	Line-to-Line voltage

V_{LN}	Line-to-Neutral voltage
V_a	Motor armature voltage
V_{dc}	DC bus voltage
$V_{iz,ref}$	i:th (i = 0, 1, 2) symmetrical reference waveform
V_o	Midpoint voltage
V_{offset}	Zero sequence voltage used in creating symmetrical references
V_{out}	Output voltage
V_{rated}	Motor rated armature voltage
e_u	Motor u-phase voltage
e_v	Motor v-phase voltage
e_w	Motor w-phase voltage
f_e	Electrical frequency
f_{rated}	Motor rated electrical frequency
f_{sw}	Switching frequency
m_a	Modulation index
$v_{i,ref}$	i:th (i = 0, 1, 2) sinusoidal reference waveform
v_{ref}	Modulator reference voltage
v_{tri}	Modulator triangular carrier voltage
ω_e	Electrical angular velocity
ω_{ref}	Electrical angular velocity reference
ω_s	Motor angular velocity
B	Motor flux density
N	Number of levels for multi-level inverter
$i(t)$	Current instantaneous value
s	Motor slip
η	Efficiency

Appendix B - Induction Motors

This appendix is streamlined version of a derivation found in [9].

The dynamic behavior of an induction motor is described by the following set of equations

$$\frac{d\vec{\Psi}_s}{dt} = \vec{u}_s - R_s\vec{i}_s$$

$$\frac{d\vec{\Psi}_r}{dt} = j\omega\vec{\Psi}_r - R_r\vec{i}_r$$

$$\vec{\Psi}_s = L_s\vec{i}_s + L_m\vec{i}_r$$

$$\vec{\Psi}_r = L_r\vec{i}_r + L_m\vec{i}_s$$

$$J\frac{d\omega}{dt} = \vec{\Psi}_s \, x \, \vec{i}_s - T_{load}$$

In this thesis a symmetrical grid with constant frequency is assumed. Under these conditions, an equivalent steady state circuit model can be derived.

All of the above equations are written in stator coordinates ($\alpha\beta$ coordinates). They are transformed to rotor coordinates (dq coordinates) through multiplication with $e^{-j\theta}$, θ being the angle between the rotating coordinate system (dq) and the stationary coordinate system ($\alpha\beta$).

$$\frac{d\vec{\Psi}_s^{dq}}{dt} = \vec{u}_s^{dq} - R_s\vec{i}_s^{dq} - j\omega_s\vec{\Psi}_s^{dq} = \vec{u}_s^{dq} - R_s\vec{i}_s^{dq} - j\omega_s\left(L_s\vec{i}_s^{dq} + L_m\vec{i}_r^{dq}\right)$$

$$\frac{d\vec{\Psi}_r^{dq}}{dt} = j\omega\vec{\Psi}_r^{dq} - R_r\vec{i}_r^{dq} - j\omega_s\vec{\Psi}_r^{dq} = j(\omega - \omega_s)\left(L_m\vec{i}_s^{dq} + L_r\vec{i}_r^{dq}\right) - R_r\vec{i}_r^{dq}$$

In addition, assuming steady state operation, the derivatives of the flux linkages are zero, reducing the equations to

$$\vec{u}_s^{dq} - R_s\vec{i}_s^{dq} - j\omega_s\left(L_s\vec{i}_s^{dq} + L_m\vec{i}_r^{dq}\right) = 0$$

$$j(\omega - \omega_s)\left(L_m \vec{i}_s^{dq} + L_r \vec{i}_r^{dq}\right) - R_r \vec{i}_r^{dq} = 0$$

The constant vectors in the equations above are recognized as phasors. Hence, in the following discussion, all vectors are replaced by phasors and the phasor $\overline{u}$ is chosen as a reference.Note that $\overline{u}$ is the RMS value of the phase voltage.

The slip is defined as $s = \frac{\omega_s - \omega}{\omega_s}$ and the frequency of the input as ω_1. Then, beginning with the rotor equation, it is seen that

$$0 = j(\omega - \omega_s)\left(L_m \bar{i}_s - L_r \bar{i}_r\right) + R_r \bar{i}_r = -js\omega_s\left(L_m \bar{i}_s - L_r \bar{i}_r\right) + R_r \bar{i}_r$$
$$= -js\omega_s L_m\left(\bar{i}_s - \bar{i}_r\right) + js\omega_s L_{r\lambda} \bar{i}_r + R_r \bar{i}_r$$

Here the equation can be divided by s and$\omega_s$replaced with ω_1

$$0 = -j\omega_1 L_m\left(\bar{i}_s - \bar{i}_r\right) + j\omega_1 L_{r\lambda} \bar{i}_r + \frac{R_r}{s} \bar{i}_r$$

This is known as the rotor equation in steady state operation. Finally, the steady state stator equation is attained by replacing ω_s with ω_1

$$\overline{u}_s = R_s \bar{i}_s + j\omega_1\left(L_s \bar{i}_s - L_m \bar{i}_r\right) = R_s \bar{i}_s + j\omega_1 L_{s\lambda} \bar{i}_s + j\omega_1 L_m\left(\bar{i}_s - \bar{i}_r\right)$$

The stator and rotor equations can now be combined to form the equivalent circuit.

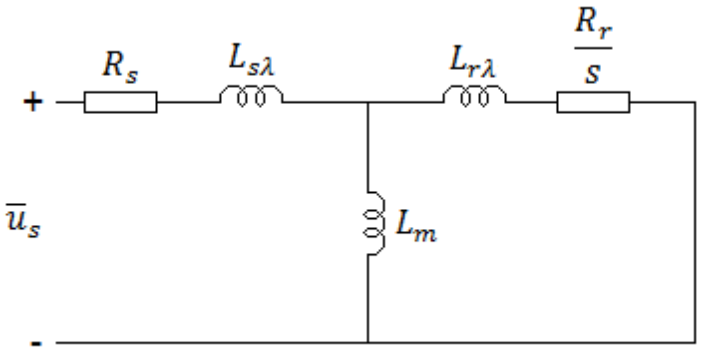

Fig B.1 Equivalent circuit for one phase of an induction motor

Appendix C - VHz Control

This appendix is streamlined version of a derivation found in [10].

In an induction motor, the synchronous angular velocity is proportional to the electrical frequency of the applied armature voltage.

$$\omega_s = (\frac{2}{\#\ poles})\omega_e$$

It is clear that one can control the induction motor speed by varying the frequency of the applied armature voltage. As discussed in the modulation section above, this is done by varying the frequency of the reference waveforms.

Faraday's law can be used to show that the applied armature voltage is directly proportional to the peak flux density and the electrical frequency.

$$\hat{V}_a = (\frac{f_e}{f_{rated}})(\frac{\hat{B}}{B_{rated}})V_{rated}$$

Thus, if the amplitude of the voltage is kept at its rated value and vary the

electrical frequency, the following is found

$$\hat{B} = \left(\frac{f_{rated}}{f_e}\right) B_{rated}$$

This means that if the electrical frequency is lowered, the flux density will increase, leading to additional core loss and increased currents, possibly damaging the motor. Hence, induction motors should operate a constant flux density.

$$\hat{V}_a = (\frac{f_e}{f_{rated}})V_{rated}$$

this expression can be rewritten as

$$\frac{\hat{V}_a}{f_e} = \frac{V_{rated}}{f_{rated}}$$

Hence, constant flux density is attained when a constant ratio of armature voltage and electrical frequency is maintained. Therefore, this type of controlled is often referred to as Volts-per-Hertz control, or VHz.